A CAHNERS PUBLICATION INTERNATIONAL EDITION FEBRUARY 5, 1987

EDN

Improving an ADC's differential linearity

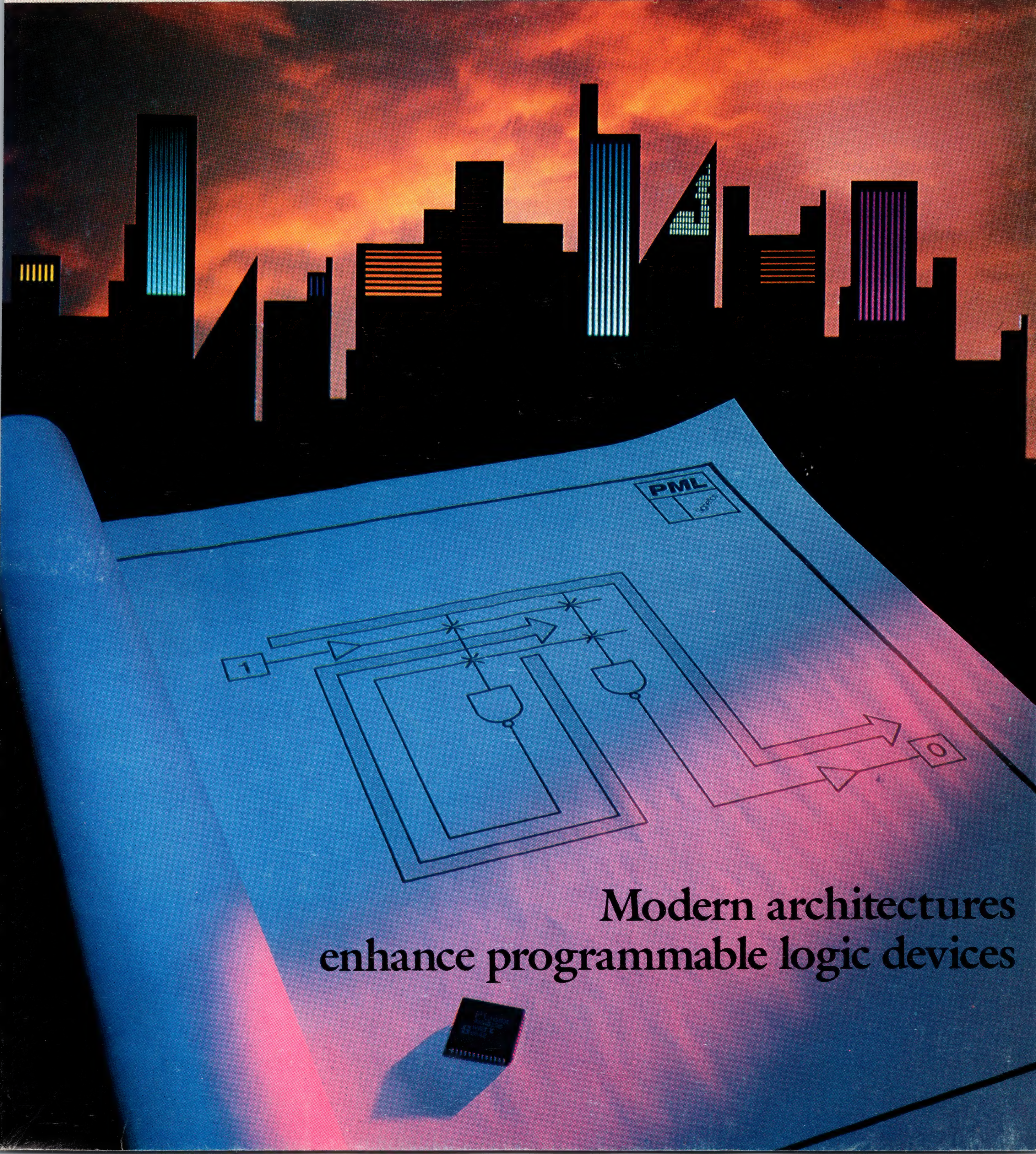
Bit-error-rate testers

Project-management software for IBM PCs

Jim Williams: Circuits as art

6 APR REC'D

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



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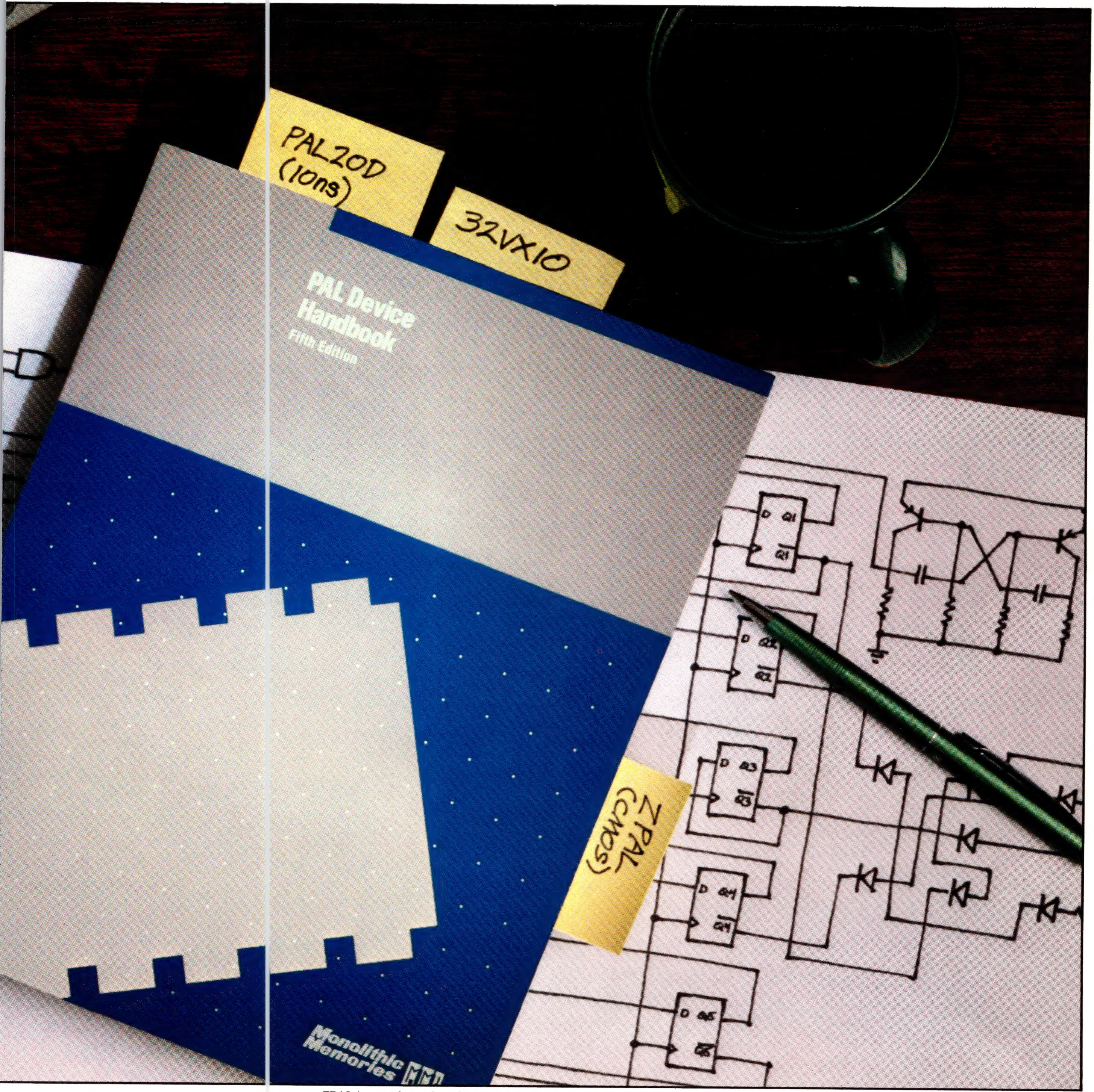

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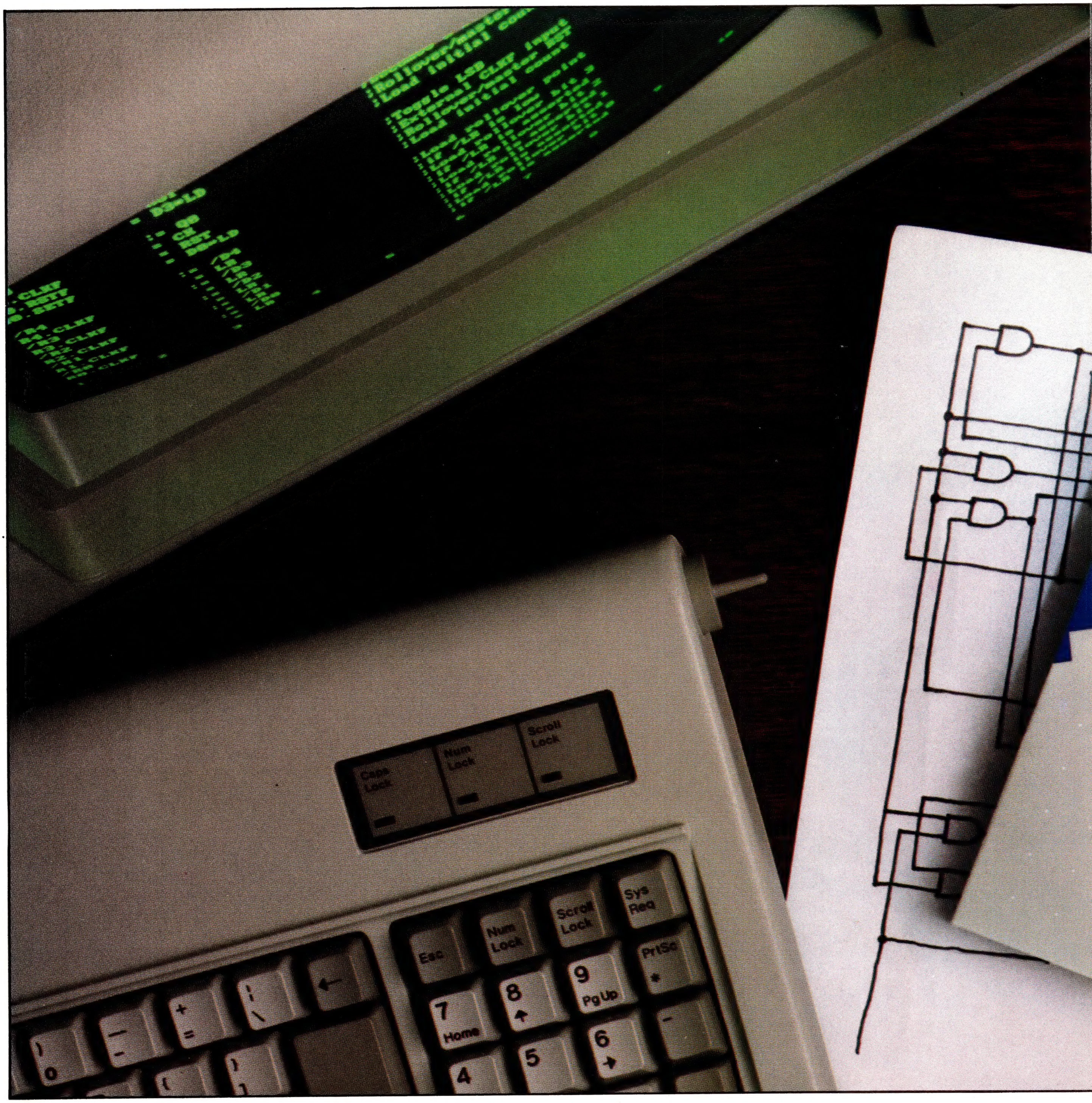
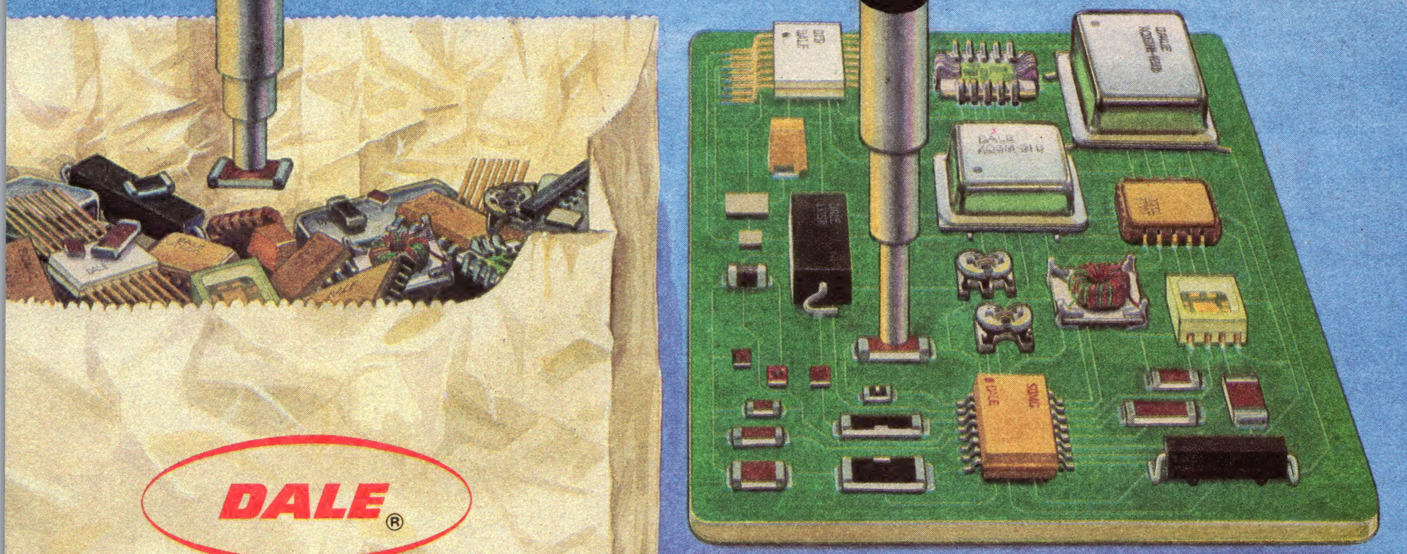


Save your system.

Pick & Place.



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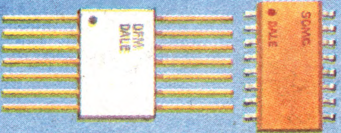
Thick Film Networks

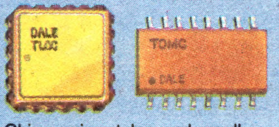
SOMC DFM DFP LCCC



Small outline molded dip package, ceramic chip carrier styles and flat pack (MIL-R-83401). All standard schematics. R/C styles available.

Thin Film Networks

TLCC TOMC



Chip carrier styles and small outline molded dip package. All standard schematics.

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Thin Film Chips

TNP
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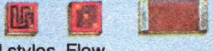
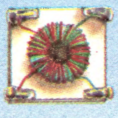


Commercial styles. Flow solderable. Single element and tapped, wire bondable.

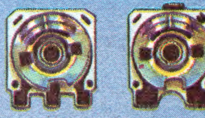
Transformers



Custom designs available.

Chip Potentiometers

ST



Standard, automatic or reverse adjustment. 100 ohms to 1 Meg.

Thermistors

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NTC style. 5% & 10%, R_{25} tolerance.

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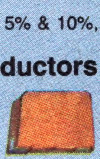
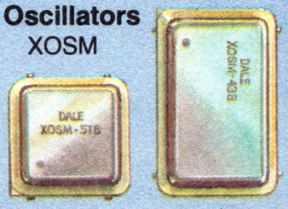


Molded style, 1 µH to 1000 µH. 10% & 20% tolerance.

Oscillators

XOSM



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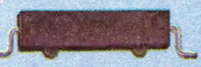

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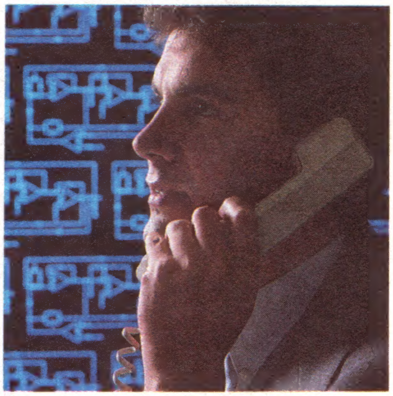

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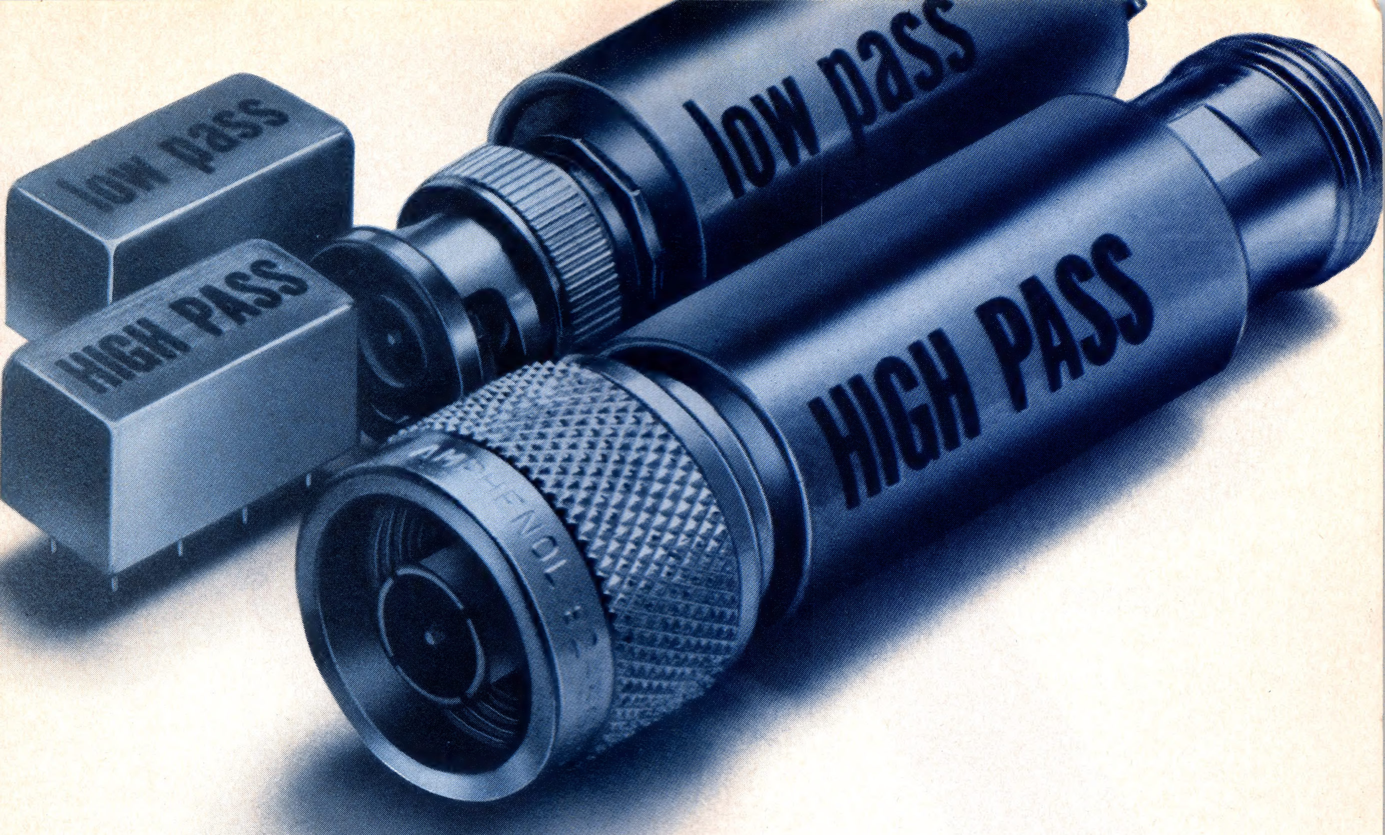

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	end, min.	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
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*Prefix P for pins, B for BNC, N for Type N, S for SMA   example: **PLP-10.7**

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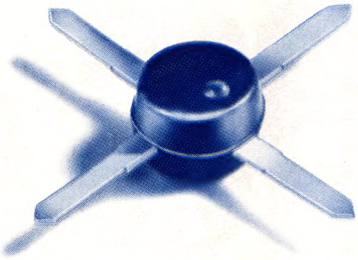

dc to 2000 MHz amplifier series

SPECIFICATIONS

Model	Frequency MHz	Gain, dB (min.)	Max. Power dBm (typ)	NF dB (typ)	Price $ Ea.	Qty.
MAR-1	DC-1000	13	0	5.0	0.99	(100)
MAR-2	DC-2000	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	8	+8	6.0	1.70	(25)
MAR-4	DC-1000	7	+11	7.0	1.90	(25)
MAR-7	DC-2000	8.5	+4	5.0	1.90	(25)
MAR-8	DC-1000	21	+10	3.5	2.20	(25)

Unbelievable, until now...tiny monolithic wideband amplifiers for as low as 99 cents. These rugged 0.085 in.diam.plastic-packaged units are 50ohm input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer from 7 to 21dB gain, 0 to +11dBm output, noise figure as low as 3.5dB (5.5dB typical), and up to DC-2000MHz bandwidth.

**3:1 load VSWR for the MAR-8*

designers amplifier kit, DAK-1

5 of each model, total 30 amplifiers

only $49.99

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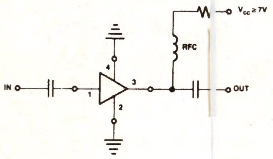
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047, .068, .1µf

* MINIMUM ORDER 50 PER VALUE

Typical Biasing Configuration



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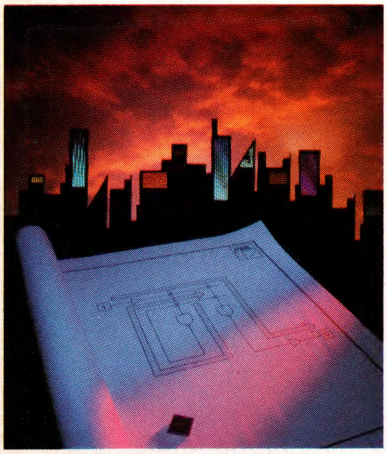
Volume 32, Number 3

EDN

February 5, 1987

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *A programmable logic device with an enhanced, more flexible architecture can replace several older devices, thus reducing the number of different devices you need to stock. The more flexible devices can also untangle knotty pc-board layout problems. See pg 112. (Photo courtesy Signetics)*

DESIGN FEATURES

Special Report: Programmable-logic devices 112

During just this past year, programmable-logic devices have made significant progress: Lower prices, increased speed, lower power consumption, new process technologies, and increased flexibility are the notable improvements. The largest PLDs are poised to enter ASIC territory.—*Charles H Small, Associate Editor*

Hardware methods improve 1-chip A/D converters 139

By using progressive clocking, a sliding-scale technique, and error-correction methods, you can improve the speed and the differential linearity of 1-chip successive-approximation A/D converters. Thus, in a given application, you can use a lower-cost A/D converter than would otherwise be possible.—*Steven Sidman and Steven Harris, Advanced Micro Devices Inc*

Knowing error sources lets you evaluate hard-disk drives 165

Because they are electromechanical parts, hard-disk drives inherently exhibit a higher failure rate than do solid-state electronic components. Understanding the sources of error in high-capacity hard-disk drives can help you institute a comprehensive program of quality assurance for your systems that use disk drives.—*George Robinson, FlexStar Corp*

Designer's guide to EDIF—Part 2 175

This article, the second of a 4-part series, shows you how to translate your semicustom libraries into the Electronic Design Interchange Format so that you can transfer the libraries to any CAE system or ASIC foundry that accepts this format. You can use EDIF to create schematic, behavioral, and physical representations of the components.—*Mike Waters, Esther Marx, and Hart Switzer, Motorola Inc*

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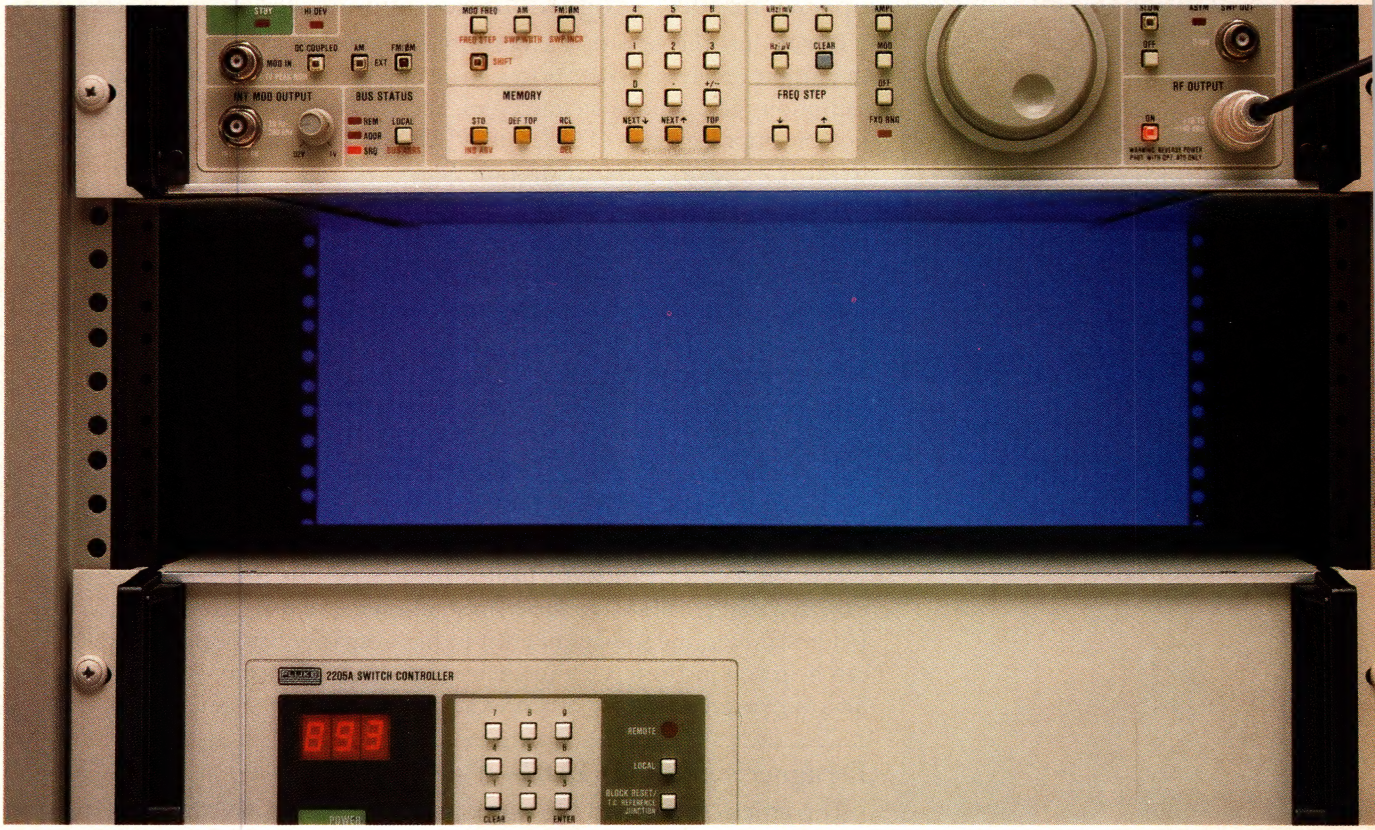

The 1722A is designed for fast system integration, right down to the size.

When you're configuring an ATE station, no computer makes integration as fast and easy as Fluke's 1722A Instrument Controller. Designed for a standard 19-inch rack, the 1722A doesn't have to be adapted to your system. It slides into your rack in seconds.

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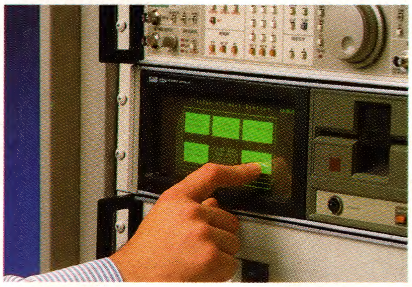

Once programmed, the touch-sensitive display replaces the keyboard for system control. The operator is prompted one step at a time and responds by simply touching the screen.

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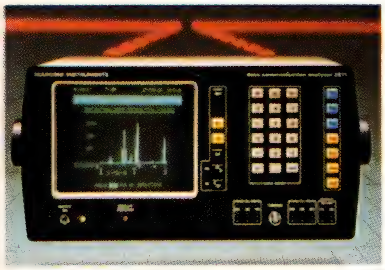
February 5, 1987



***General-purpose bit-error-rate testers** can help you evaluate the data-transmission capabilities of twisted-pair wiring, coaxial cable, fiber-optic cable, or radio links (pg 69).*

TECHNOLOGY UPDATE

Project-management software for PCs helps you map out a plan for your project 57

If you're responsible for managing a project from start to finish, you can use a personal computer and a software project-management package for activity planning, scheduling, and tracking.—*Steven H Leibson, Regional Editor*

Bit-error-rate testers troubleshoot data links in real time 69

When you're networking data over a wide-area network—such as a public switched telephone network, leased phone lines, or a packet-switching network—it's important that the data links you use meet their published performance figures. To find out whether they do, you can use bit-error-rate testers.—*Peter Harold, European Editor*

ISSCC '87 will explore IC design in a restructured semiconductor industry 85

The shift in the semiconductor industry will bring about a shift in the traditional role of the IC designer, maintains Robert Brodersen, the keynote speaker at this year's International Solid State Circuits Conference, which will take place February 25 through 27 in New York, NY.—*David Shear, Regional Editor*

PRODUCT UPDATE

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Board for IEEE-488 instrument control 100
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It is worth the effort to set clear goals and keep yourself aimed at them throughout any project.

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Jim Williams: Circuits as art.—*Deborah Asbrand, Associate Editor*

LOOKING AHEAD 249

Analysts' 1987 forecasts vary for US semiconductor sales. . . Async dial modems stay on top in units shipped to 1991.

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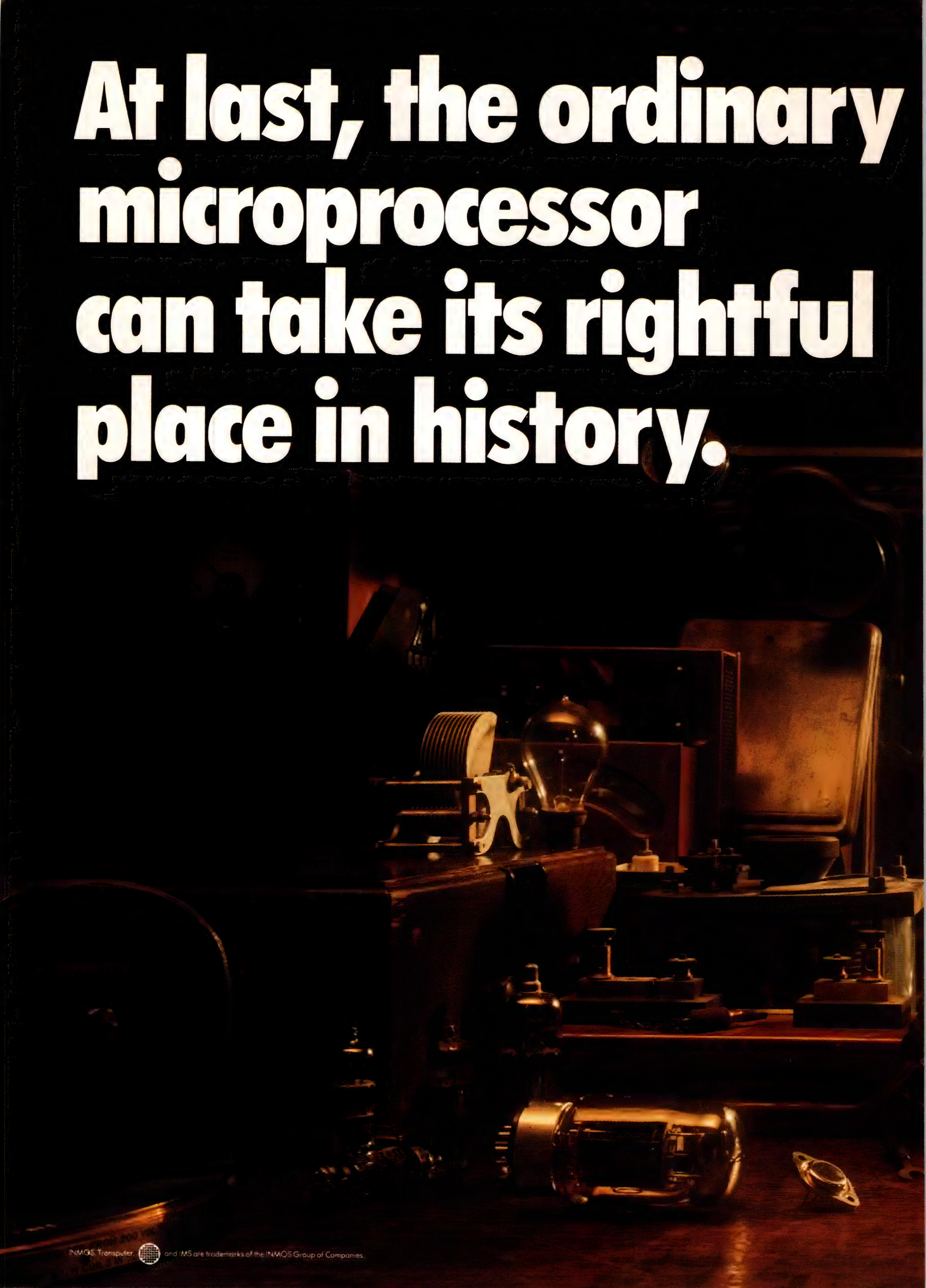
At last, the ordinary microprocessor can take its rightful place in history.

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It had to happen—the conventional microprocessor has had its day. Relegated to the ranks of yesterday's devices by the new transputer family from INMOS. It's history in the making.

The IMS T414 transputer is a fast, easy-to-use VLSI component, integrating a 32-bit processor, four inter-transputer communication links, 2K bytes Static RAM, 32-bit memory interface and DRAM controller. All on a single CMOS chip—offering execution rates up to 10 MIPs.

While transputers excel in single-processor systems, their real power can be unleashed by connecting any number of transputers together via the high-speed serial links. Multi-transputer systems can deliver the performance you need today, and can be easily expanded in the future as your processing requirements increase.

And there's more. Programming multiprocessor systems has never been easier. The Transputer Development System (TDS) supports C, Fortran, Pascal and OCCAM, providing a complete software development environment, and is available for a number of popular hosts. Software developed on the TDS can be executed on one or more transputers, enabling cost-performance tradeoffs to be made.

INMOS transputers are available now and have already found their way into companies who are evaluating, prototyping and manufacturing transputer-based systems. Applications include supercomputers, DSP, graphics, robotics, AI, distributed control systems, PC's, engineering workstations and many others.

Write or phone for more information on the transputer family and start making history yourself.

TRANSPUTER PRODUCTS	
IMS T414	32 bit Transputer—2Kbyte —4 links
IMS T212	16 bit Transputer—2Kbyte —4 links
IMS M212	16 bit Disc Processor—1Kbyte—2 links
DEVELOPMENT TOOLS	
IMS D701-2	IBM PC—Transputer Development System.
IMS D600	VAX/VMS—Transputer Development System.
EVALUATION BOARDS	
IMS B002-2	Double Eurocard + IMS T414 + 2Mbyte DRAM + 2 x RS232.
IMS B003-1	Double Eurocard + 4 x IMS T414 + 4 x 256Kbyte DRAM.
IMS B004-2	IBM PC Format + IMS T414 + 2Mbyte DRAM.
IMS B006-2	Double Eurocard + 9 x IMS T212 + 128Kbyte SRAM.
IMS B007-1	Double Eurocard + IMS T414 + 0.5Mbyte DRAM + 0.5Mbyte Video RAM.
HIGH PERFORMANCE VLSI MEMORIES	
16K CMOS SRAM, 25-45ns, 64K CMOS SRAM, 35-70ns 256K CMOS DRAM, 60-100ns	

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CIRCLE NO 115

Easy

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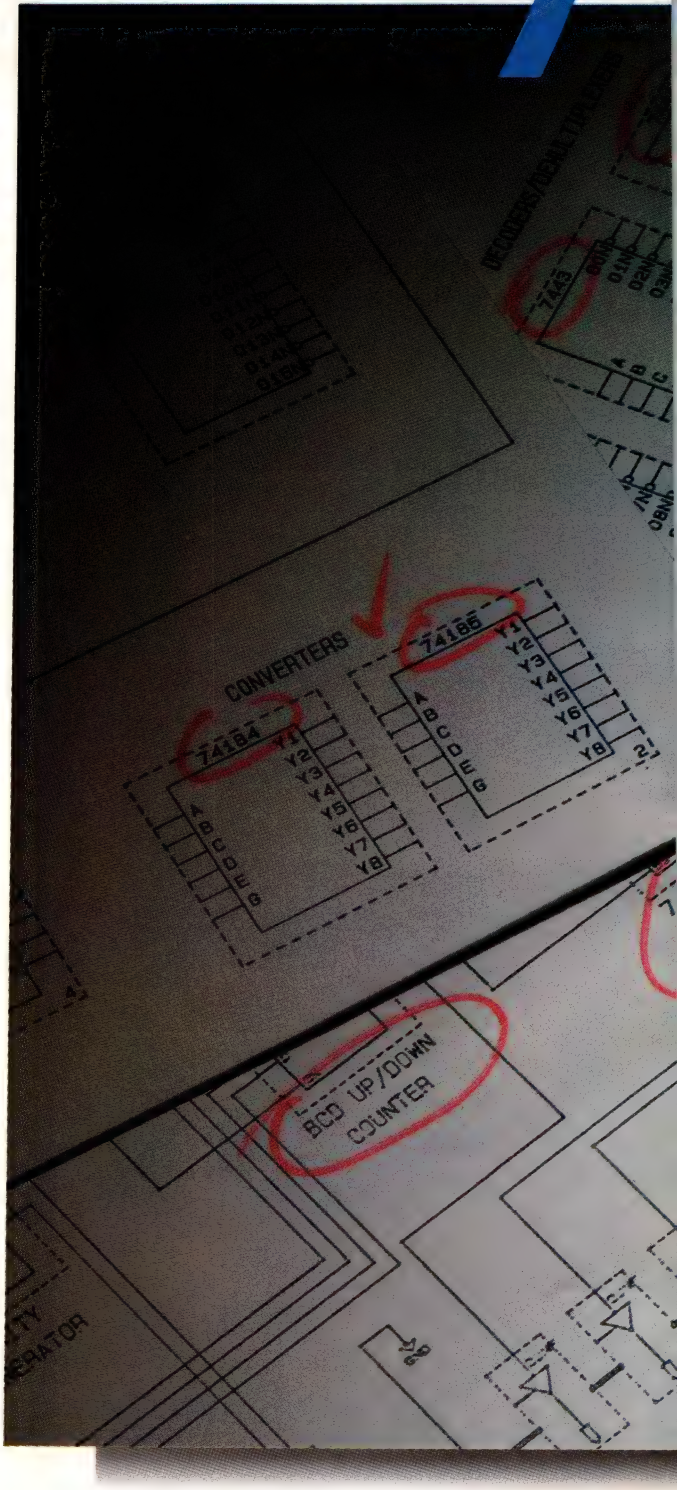

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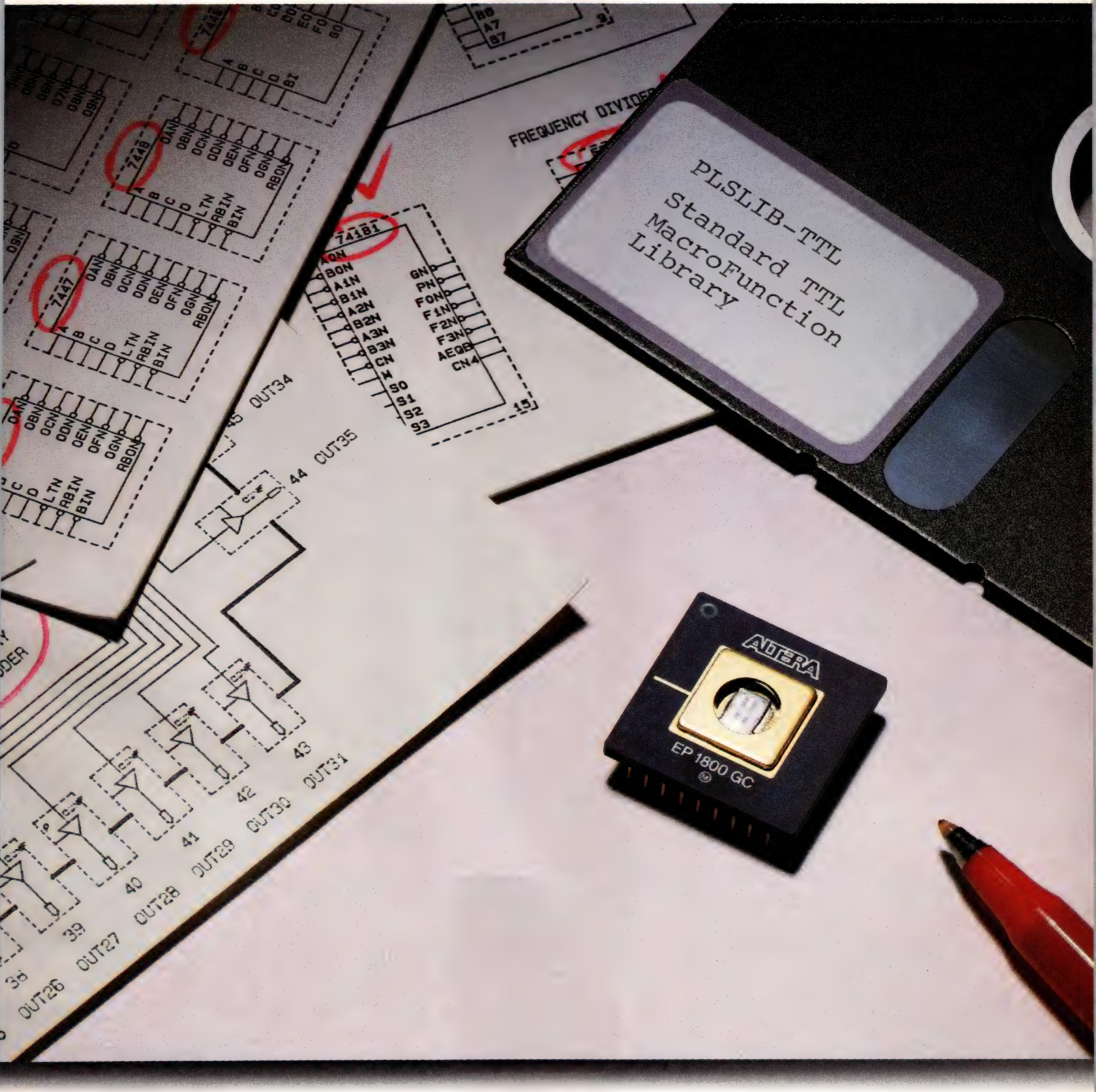

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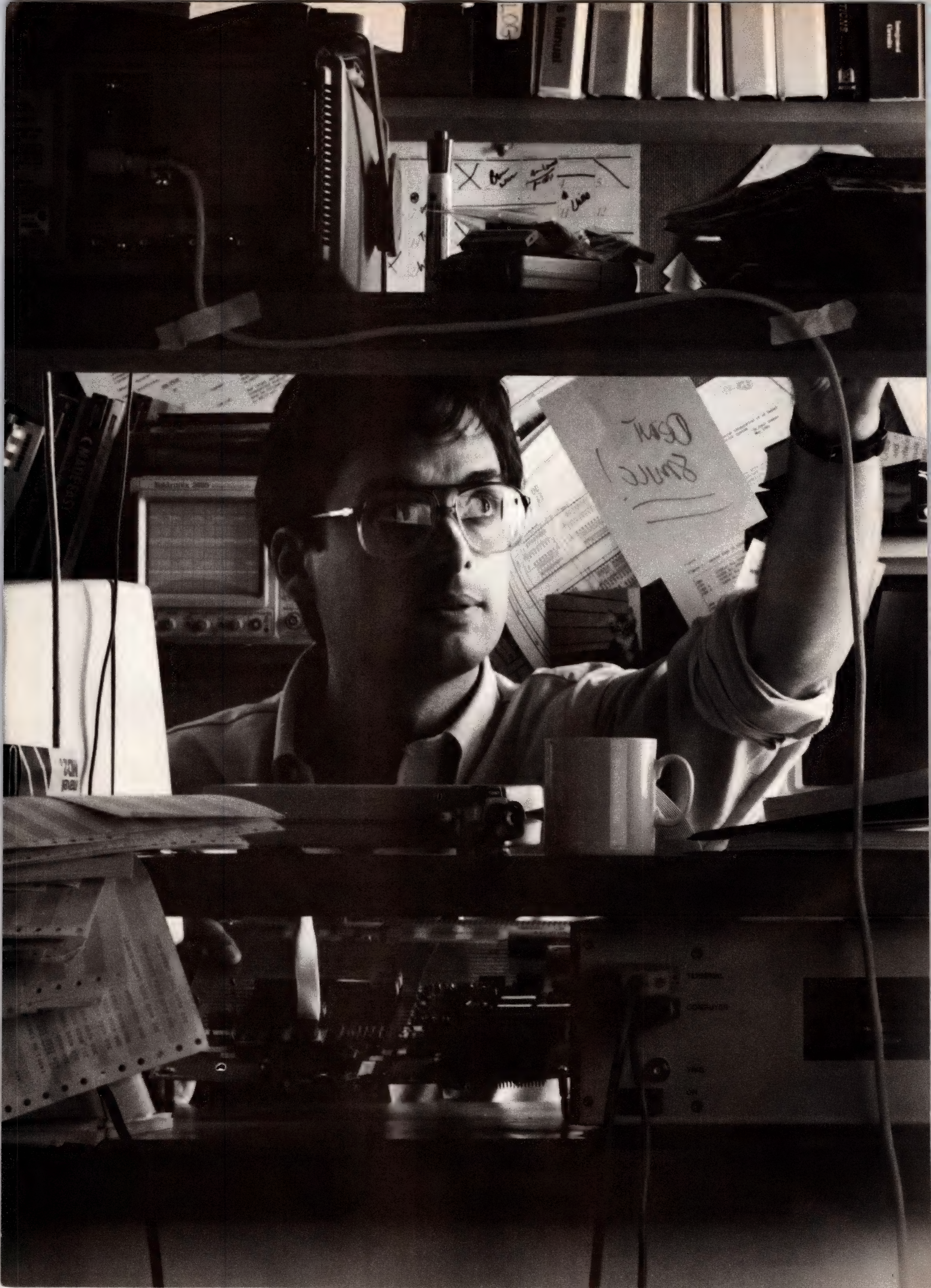


The difference between a few more tweaks and a few more weeks.

HOSTS	OPERATING SYSTEMS	TARGETS	LANGUAGES	TOOLS
VAX MicroVAX UNIX-oriented workstations · Apollo · Sun · IBM AT MS-DOS workstations · PC · PC XT · PC AT	VMS ULTRIX UNIX XENIX MS-DOS	8048 family 8080, 8085, 8086/88, 80186/188 and 80286 68HC11, 6800/2/8, 6809/9E, 68000/8/10 and 68020 Z80, MK3880/4 and Z8001/2/3 NSC-800	C Pascal FORTRAN PL/M Assembler	Assemblers Linkers Locaters Compilers Symbolic debuggers Source-level debuggers Emulators

A stand-alone or host-control system of fully integrated debug tools built on high performance emulation.

Introducing the CIDS method from Applied Microsystems. The first painless way to assemble the debug environment you really need.

You could spend weeks looking for the right tools, plus months trying to make them work together, and still not have a system that was truly integrated. That's why Applied Microsystems has developed the CIDS method.

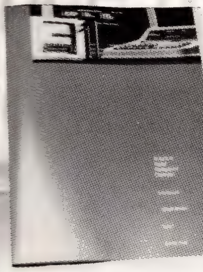
CIDS stands for Customer Integrated Development Systems and the concept is simple. You choose your hardware and software tools. Applied Microsystems makes sure they work together seamlessly.

An overview of Customer Integrated Development Systems.

Whether you're working on an 8-bit, 16-bit or even a 32-bit design, we let you tailor the emulation and debug tools you need. Everything from symbolic and source-level debuggers to assemblers, cross-compilers and utilities. The chart gives you some idea of the power and convenience of the CIDS method, but it can only hint at the control and visibility you will enjoy.

Validate™ links emulation with source-level debugging.

When your software engineers only speak C and your emulator only speaks assembler, your tools are worthless. Or if your function is in assembler and your debugger only speaks C, it's the same dead end.



The power of the Validate environment is that it works equally in high level languages and in assembler. You don't sacrifice any power or comfort.

Real-time emulation for the 68020 and 80286.

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Discover why the CIDS method is the fastest, easiest way to start and finish a design project. For technical and application details call 1-800-426-3925. In Washington state call (206) 882-2000.

Or write Applied Microsystems Corporation, P.O. Box 97002, Redmond, WA 98073-9702.

In Europe: Applied Microsystems, Brooke House, Market Square, Aylesbury, Buckinghamshire, HP20 1SN, England. Tel: 44 (0296) 34822.

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Which means:

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- **more system reliability**
  because there are less devices in the system
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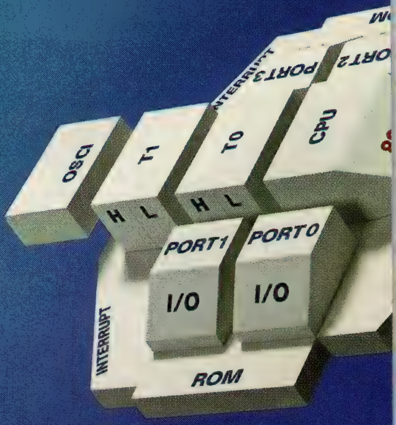
Benefits that make you more competitive, with SAB 80515/535 you're on the market faster with the better product.



Major features of SAB 80515/535:

All 8051 characteristics with twice the RAM/ROM capacity, hardware/software compatible; 12 interrupt sources/4 priority levels, 6 x 8-bit I/O ports; A/D converter with 8 inputs, S & H, 8-bit resolution; 3 x 16-bit timer/counters; 4 x 16-bit capture/compare/reload functions; watchdog timer; PLCC68 package.

Get the full details. From Siemens AG, Infoservice, Postfach 23 48, D-8510 Fürth, West Germany.

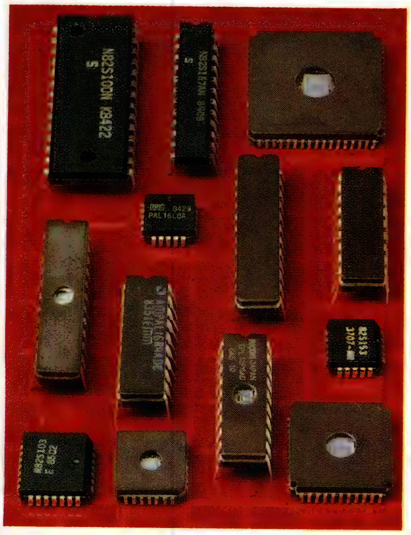
12/Z001.101

CIRCLE NO 118

80515
RAM
PORT3
PORT4
PORT5
CPU
UART
4800/9600
T0
T1
H
L
PORT1
PORT0
I/O
I/O
RAM
ROM
80515
8052
ROM
PORT2
PORT3
RAM
INTERRUPT
CPU
UART
T1
T0
H
L
H
L
OSCI
RCAP2L
RCAP2H
T2
H
L
H
L
PORT1
PORT0
I/O
I/O
RAM
INTERRUPT
ROM
8052
RAM

ZL30A

Power in design Speed in production



Stag's ZL30A offers total PLD programming support

Stag Microsystem's model ZL30A is the first dedicated Logic Programmer of its kind that not only supports programming of PLDs, EPLDs, and GALs*, in a variety of 20, 24, 28 and 40 pin DIP, but also supports programming of the latest surface mounted PLCC/LCC devices.

Stag's ZL30A contains features that have made it the industry standard in both engineering and production environments. Salient among these are:

- Powerful easy-to-use editing capability
- Super fast programming speed
- Stand alone or remote control operation
- Comprehensive device library
- Handler interface capability to support DIP or PLCC/LCC devices
- I/O formats include JEDEC, Signetics and X-Plot
- Compatible with CUPL* software compiler
- RS232C, IEEE-488 and handler control interface ports standard
- Expansion modules accommodate 40 pin DIP and a range of surface mounted devices
- Stringent in-program checks including continuity and connect tests are automatically performed to guarantee error free stand alone or handler operation
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*CUPL is a trademark of Assisted Technology

CIRCLE NO 119

NEWS BREAKS

EDITED BY JOAN MORROW

CACHE RAM SPORTS ON-CHIP COMPARATOR, HAS 20-nSEC ACCESS TIME

Suitable for use in cache tag applications, a 4k×4-bit static RAM—the MK41H80 Tagram—contains a 4-bit comparator that compares RAM contents to current input data in as little as 12 nsec. This rate translates into a 30% speed improvement over cache RAMs using external comparator circuits, according to the manufacturer, Thomson Components-Mostek Corp (Carrollton, TX, (214) 466-6000). A Flash Clear feature lets you clear all RAM bits to a logic zero in 40 nsec or less. The Tagram also provides full-speed read access to the RAM contents. You can order the Tagram with an address access time and match access time as low as 20 nsec. Other versions spec 25- and 35-nsec access times. Available in a 22-pin, 300-mil plastic or ceramic DIP, the Tagram costs $10.19 to $22.50 (100).—J D Mosley

PROGRAMMABLE FREQUENCY SYNTHESIZER OFFERS 20- TO 31-MHz RANGE

Needing no external filters or phase-locked-loop (PLL) components, the $195 FS-30 is a digitally programmable CMOS frequency synthesizer housed in a 2.25×1.6×0.5-in. shielded package. Manufactured by Analytic Instruments (Dallas, TX, (214) 357-3882), the FS-30 can drive a 25-mA load and runs from a 5V power supply. An on-chip circuit filters incoming power for stability and noise reduction. Worst-case power consumption is 120 mA over 0 to 180°F.

You must supply an external crystal or clock oscillator, but the FS-30 contains an internal PLL, a voltage-controlled oscillator, and 4-bit address and data buses. You can program the output frequency to a resolution as fine as 8192 steps/octave over a 9-decade range. The FS-30 also features a 3-state output that facilitates remote disabling via the hybrid's D register. Automatic test equipment can use this feature to disable the system clock for forced-node testing, or you can bus multiple FS-30s onto one clock line.—J D Mosley

IEEE NAMES RUSSELL DREW AS 1987 PRESIDENT-ELECT

The IEEE has announced Russell Drew as its 1987 president-elect. The formal announcement of the election's winner was delayed for one month while an IEEE committee reviewed an election challenge that had been filed by another candidate, Irwin Feerst. Feerst lost the election by 242 votes. The IEEE Credentials Committee reviewed Feerst's complaint and issued a statement that it found no evidence indicating there had been a violation of the IEEE's constitution, bylaws, or policies and procedures.

Drew is president of Viking Instruments, a Sterling, VA, manufacturer of analytical instruments. He will serve as IEEE president-elect in 1987 and as the organization's president in 1988.—Deborah Asbrand

COMPANIES REDUCE PRICES OF TAPE SUBSYSTEMS, VIDEO TERMINALS

Tallgrass Technologies Corp (Overland Park, KS, (913) 492-6002) has reduced the prices of its tape and disk-tape subsystems by as much as 45%. For instance, the $895 Model TG-1020i (20M-byte internal tape) now costs $495; the $2295 Model TG-2025e (external 20M-byte tape with 25M-byte hard disk) sells for $1595; and the Model TG6180 (external 60M-byte tape with 80M-byte hard disk) was $7660 and now costs $4995. Similarly, the Computer Products Div, Apmex Corp (El Segundo, CA, (213) 640-0150) has scaled down the price of its 220 video display terminal from $649 to $529.—Joan Morrow

NEWS BREAKS

ATE SYSTEM HANDLES SMART-POWER DEVICES

Teradyne Inc (Boston, MA) has added options to its A360Z analog-LSI test system that enable it to test smart-power devices. The M644 ($65,000) and M648 ($70,000) smart-power option packages test devices that integrate control and power circuits. The M644 version features dual high-power channels, a single high-voltage channel, and 12 digital channels. The M648 package has dual high-power channels, one high-voltage channel, and eight digital channels.—Charles H Small

VME BUS INTERFACE PROVIDES TWO INDEPENDENT SCSI PORTS

If you want to add SCSI peripherals to your VME Bus system, you can use the V/SCSI 4210 host adapter from Interphase Corp (Dallas, TX, (214) 350-9000). It provides two independent SCSI ports that accommodate as many as 14 devices communicating at 1.5M-byte/sec asynchronous and 4.0M-byte/sec synchronous data-transfer rates. Each port facilitates the full Common Command Set and a variety of vendor-specific commands. You can also use the 4210 host adapter for intercomputer connections. Its proprietary BUSpacket interface fosters 30M-byte/sec DMA data rates by decoupling VME Bus activity from on-board processes and SCSI bus activity. Other features include a real-time multitasking kernel, command queuing, command order optimization, a virtual buffer architecture, a 68000 μP, and a 128k-byte cache buffer. The 4210 costs $1750 (100).—J D Mosley

4-CHANNEL TRACK/HOLD IC SPECS 1-μSEC ACQUISITION TIME

The CS31412 uses on-chip digital calibration to achieve 12-bit precision. Developed by Crystal Semiconductor (Austin, TX, (512) 445-7222), the IC is a 4-channel simultaneous track/hold circuit on a monolithic chip. Suitable for a variety of signal-processing applications that require simultaneous sampling, the CS31412 consists of four track/hold amplifiers, a multiplexer, and two output buffers. An on-chip μP interface allows software-controlled channel selection and calibration. This IC specs a total unadjusted error of 700 μV. An autocalibration feature ensures accuracy. Packaged in an 18-pin ceramic DIP, the CS31412 operates from a 5V power supply, dissipates 250 mW of power, and costs $36 (100). An evaluation board that allows simulation of the CS31412's performance in dynamic environments is available for $100, including a socketed CS31412.—J D Mosley

TECHNOLOGY AGREEMENT TO COVER USER-CONFIGURABLE ICs

Altera Corp (Santa Clara, CA) and WaferScale Integration Inc (Fremont, CA) have signed a 5-year technology-exchange agreement that should make new user-configurable logic devices available in the first half of this year. Altera will provide architecture, circuit-design, and software support for the new family; WaferScale will take care of the high-speed CMOS process and EPROM development.—Joan Morrow

BUS EXPANDER/ISOLATOR CONNECTS TWO IEEE-488 BUS SYSTEMS

The GPIB-120 bus expander/isolator from National Instruments (Austin, TX, (800) 531-4742 or (800) 433-3488) lets you connect 29 devices to an IEEE-488 bus by linking two systems, thus increasing the available cable length. You can use multiple GPIB-120s to access additional devices. This $995 unit also isolates instruments from the controller, thereby solving measurement problems when making small-signal measurements or when operating in noisy environments. For ease of use, the unit has no switches to set, and its operation is transparent to application software. The GPIB-120 detects the location of controllers, talkers, and listeners, and it configures itself. Front-panel LEDs let you monitor bus operations.—J D Mosley

MESSAGE CENTER DISPLAY SYSTEMS

W424 4040 4X40	W424 105D 1X5D	W424 105B 1X5B		W424 1058	W424 1053	W424 1051
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●	●	●	Enclosed in Metal Housing			
●	●	●	NEMA 12 or 4X Stainless Steel Bezel			
●	●	●	115/230 Volt Power Supply Included			
			12 Volt Power Supply Required	●	●	●
●			Four Line x 24 Character Readout			
	●	●	Single Line Readout (24 Characters)	●	●	●
			64 Canned Messages in EPROM	●		
●	●		256 Canned Messages in CMOS RAM			
●	●	●	½" Characters Utilizing Gas Plasma Technology	●	●	●
●	●		RS232/RS422 and 20mA Outputs			
			Full and Half Duplex Communication		●	
●	●	●	Accepts RS422 Serial ASCII Input			
●	●	●	Accepts RS232 & 20mA Serial ASCII Input		●	●
●	●		PC Software Available for Message Programming			
●	●	●	Accepts Parallel ASCII Input (TTL Logic Levels)		●	●
●	●		Recall Message with +5 to +30VDC Logic			

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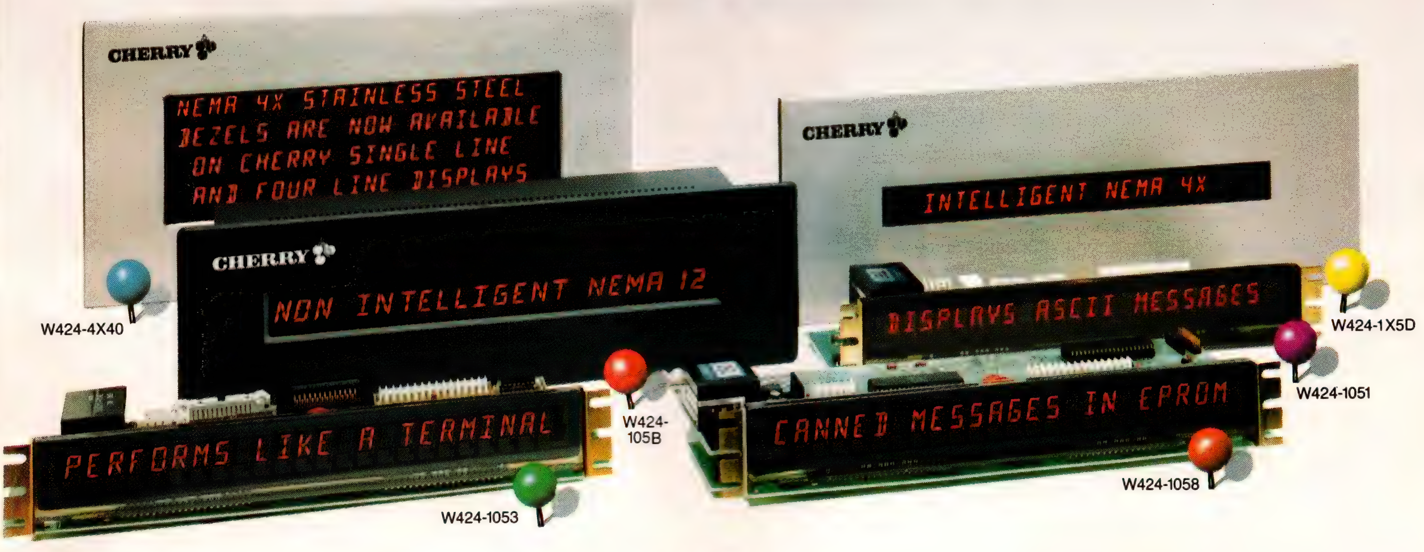

CIRCLE NO 120

NEWS BREAKS: INTERNATIONAL

HYPER-RED LEDS PRODUCE 200 mcd WITH 10-mA DRIVE CURRENT

Refinements in the passivation technique used to manufacture these hyper-red LEDs from Philips's Elcoma Div (Eindhoven, The Netherlands, TLX 51573) gives them a high percentage of aluminum in their GaAlAs epitaxial layers. The resulting high electron-injection efficiency allows the LEDs to produce luminous outputs as high as 200 mcd when driven with a current of 10 mA. In addition, you can drive the LEDs with currents as high as 1A without seriously affecting their lifetimes.

The high aluminum content also shifts their radiated output from the wavelength of between 660 and 670 nm typical of competitor's devices, to a wavelength of 650 nm. At 650 nm, the human eye is more sensitive to red light, so the Philips LEDs also appear brighter for a given luminous output. In volume, these hyper-red LEDs sell for around Gld 0.225 to Gld 0.275 each.—Peter Harold

PORTABLE HARD-DISK DRIVES PROVIDES 10M BYTES OF STORAGE

The NDK10D from Nippon Denso Kogyo was designed for Nippon Electric's PC9801 personal computer. The drive, which fits in the palm of a hand, features a 3½-in. disk that's hermetically sealed into the box. It provides 10M bytes of storage capacity, weighs 850g, and measures 106×146×31 mm. A ¥52,000 ($325) adapter connects the hard-disk drive to the personal computer. The NDK10D costs $700.—Joan Morrow

SINGLE-CHIP PWM CONTROLLER DRIVE 3-PHASE OUTPUT STAGES

Suited to the control of 3-phase variable-speed ac motors, dc brushless motors, or PWM converters, the MA818P waveform generator IC from Marconi Electronic Devices Ltd (Lincoln, UK, TLX 56380) includes all the logic necessary to produce 3-phase PWM output signals. The chip controls three complementary electronic switch pairs, which may be MOSFET, bipolar, or GTO thyristor devices. You can program delays into the output waveforms to maximize the efficiency of the complementary switching.

The waveform generator is configured via a μP interface. It accepts constant carrier frequencies in the range 600 Hz to 19.5 kHz and has user-selectable power frequency ranges of 0 to 50 Hz and 0 to 3 kHz. You can define the shape of the power frequency's waveform with data contained in an external ROM. The MA818P costs £20 (100) or £10 in high volume.—Peter Harold

SINGLE-CHIP DISPLAY CONTROLLER HANDLES FOUR DISPLAY TYPES

A joint venture between Nippon Gakki Co and software manufacturer ASCII has resulted in a single-chip display controller that can handle any of the four types of displays—CRT, electroluminescent, plasma, and liquid crystal. The CMOS device is compatible with IBM's MDA, CGA, and HGC displays. Nippon Gakki will produce the ¥6000 ($37.50) device; both companies will sell it.—Joan Morrow

256k-BIT STATIC RAM HAS 35-nSEC ACCESS TIME

The Model μPD43254C from Nippon Electric Co is a 64-word×4-bit device that provides a 35-nsec access time. Fabricated using 1.3-μm design rules and low-resistance, double-layer aluminum interconnection, the CMOS memory comes in a 300-mil, 24-pin plastic DIP. Samples sell for ¥10,000 ($62.50).—Joan Morrow

VHF scopes with something to remember!

Philips introduce another hi-tech first to remember: real-time VHF oscilloscopes (PM 3286/175 MHz & PM 3296/350 MHz) with an internal memory for up to 25 preprogrammable settings! And as selection is by means of a handheld IR control unit – **at any distance up to 7.5 m (25 ft) – you get full remote control without having to use a separate controller.** Designed for production and quality control applications, these new instruments are also ideal for measurement set-ups in hazardous or restricted-access areas. You can even remotely operate the intelligent Auto-Set beam finding facility on each scope. So in addition to a large internal memory, Philips' VHF scopes feature benefits that'll give you something more to remember!

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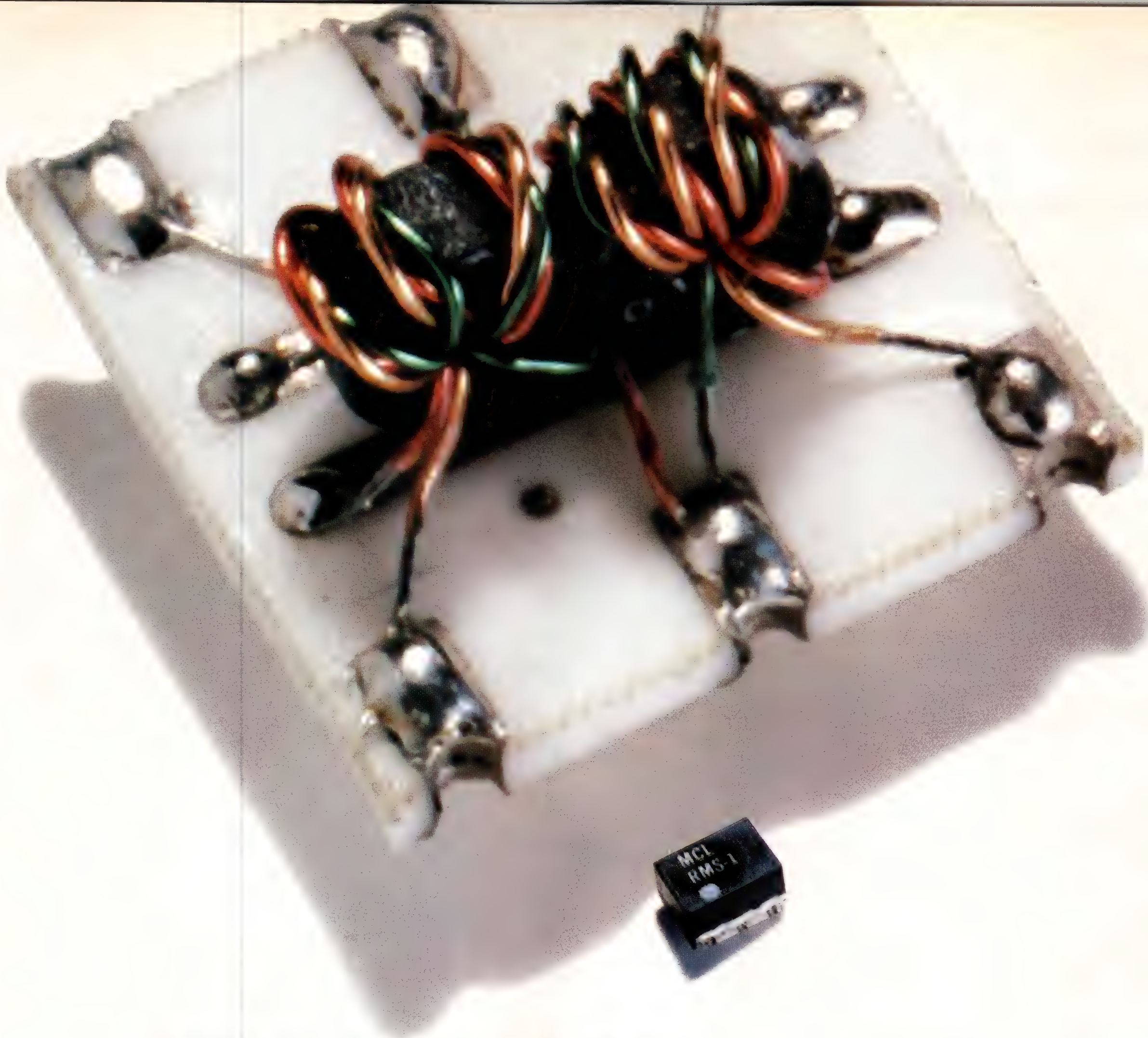

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IF		DC — 500		DC — 500	
CONVERSION LOSS, dB, Typ.					
Mid-band	($10f_l$ — $f_{u/2}$)	5.5		6.5	
Total range	(f_l — f_u)	6.2		7.0	
ISOLATION, dB, Typ.		L-R	L-I	L-R	L-I
Low-band	(f_l — $10f_l$)	55	50	55	50
Mid-band	($10f_l$ — $f_{u/2}$)	33	30	35	30
Upper-band	($f_{u/2}$ — f_u)	27	24	25	20
PRICE (10-49)		**$6.95**		**$7.95**	

f_l = lowest frequency in range

f_u = highest frequency in range

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C71 Rev. Orig.

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We've made it easy for you to write your best-selling design.

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And you can count on our ASICs specialists for technical support from design through production. One other thing you can count on with GE/RCA: there are no hidden charges in addition to your NRE.

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GE/RCA has been the CMOS company since the day we invented the technology. We've produced one best-selling CMOS circuit after another. And built the industry's broadest line of High-Rel CMOS parts, including super radiation-hardened Silicon-on-Sapphire.

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Bring 32 bit 80386 power to your existing software. Or upgrade your 68000 designs to 25 MHz speeds. Both with no-wait-states. You now have the choice between the two most powerful 32 bit micros on the industry leading VMEbus. Check the best product for your application.

Force 32 bit CPU Availability

	CPU-20	CPU-21	CPU-24	CPU-25	CPU-386A	CPU-386B
Processor	68020*	68020*	68020*	68020*	80386*	80386*
Available frequencies	12.5/16.7/ 20/25	12.5/16.7/ 20/25	12.5/16.7/ 20	12.5/16.7/ 20	12/16/20	12/16/20
Number of wait states	0	0	1	1	0 (1 at 20 MHz)	
FPU	no	yes	no	yes	no	yes
MMU	no	no	yes	yes	yes	yes
Memory capacity	0.5 to 4 MB SRAM		0.5 to 4 MB SRAM		2 to 8 MB DRAM	
EPROM capacity	512 KB	512 KB	64 KB	64 KB	256 KB	256 KB
Serial I/O channels	3	3	3	3	3	3

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CIRCLE NO 47

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SIGNALS & NOISE

Conscionable career choices aren't easy

Dear Editor:

After reading Pete Simmons's letter in the October 2 issue of EDN (pg 30), I feel compelled to write to you to question Mr Simmons's view of the proper choice of career objectives. I wonder how Mr Simmons formulates his ideas on the Nicaraguan government's use of computers. Has he spoken to anyone who has visited Nicaragua? Does he in fact know that the government there is using computers to track down dissidents in order to torture them? I have spoken to programmers who have gone to Nicaragua as part of TecNica's program and they led me to believe that nothing of that sort is going on there.

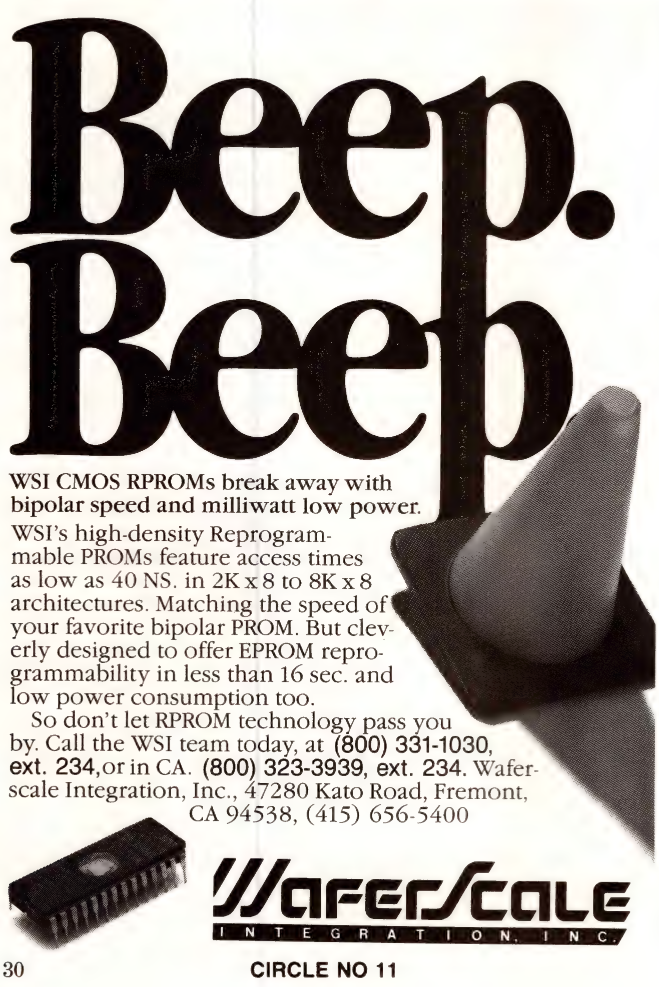
In a more general vein, I wonder at the logic of Mr Simmons's letter. The choices technical professionals have to make with regard to the types of projects they work on will never be simple black-and-white decisions. Mr Simmons's implication that data-processing equipment used to "keep track of dissidents and malcontents" is in fact military weaponry is a bit farfetched. By the same logic, one might insist that anyone working at a plant that manufactures pencils that are sold to the Pentagon should find another place to work if he has qualms about putting his life's efforts into military work. My point is that very few areas of technical work are completely removed from military work, but people who don't wish to work on military systems must draw the line somewhere.

A reasonable way to do so might be to examine the primary use of the project you're planning to work on. For example, a computer you design may be used in the military, but it may also end up in educational or medical environments. The primary purpose of missile-guidance systems is easier to classify. Each individual has to examine his own beliefs and options and act as he sees fit, but I certainly think such decisions deserve some lengthy and honest thought.

Finally, I think Mr Simmons's statement that these decisions should be made in an environment that's free of ideological considerations is ridiculous. A person's ideology is likely to be the strongest factor in determining what sort of work he or she pursues or rejects. These beliefs are the checks built into our free society, checks that will hopefully prevent an individual's greed from driving him to pursue interests that would be harmful to society as a whole.

Mr Simmons's statement about Nicaragua makes it clear that he himself is not considering your July

Text continued on pg 34



WSI CMOS RPROMs break away with bipolar speed and milliwatt low power.

WSI's high-density Reprogrammable PROMs feature access times as low as 40 NS. in 2K x 8 to 8K x 8 architectures. Matching the speed of your favorite bipolar PROM. But cleverly designed to offer EPROM reprogrammability in less than 16 sec. and low power consumption too.

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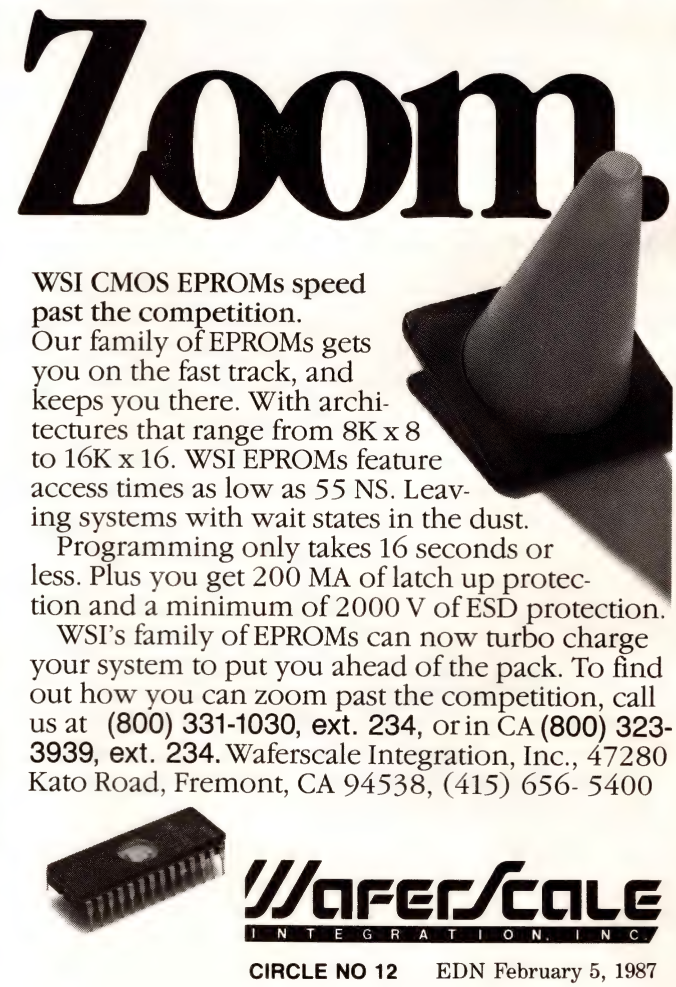

WSI CMOS EPROMs speed past the competition.

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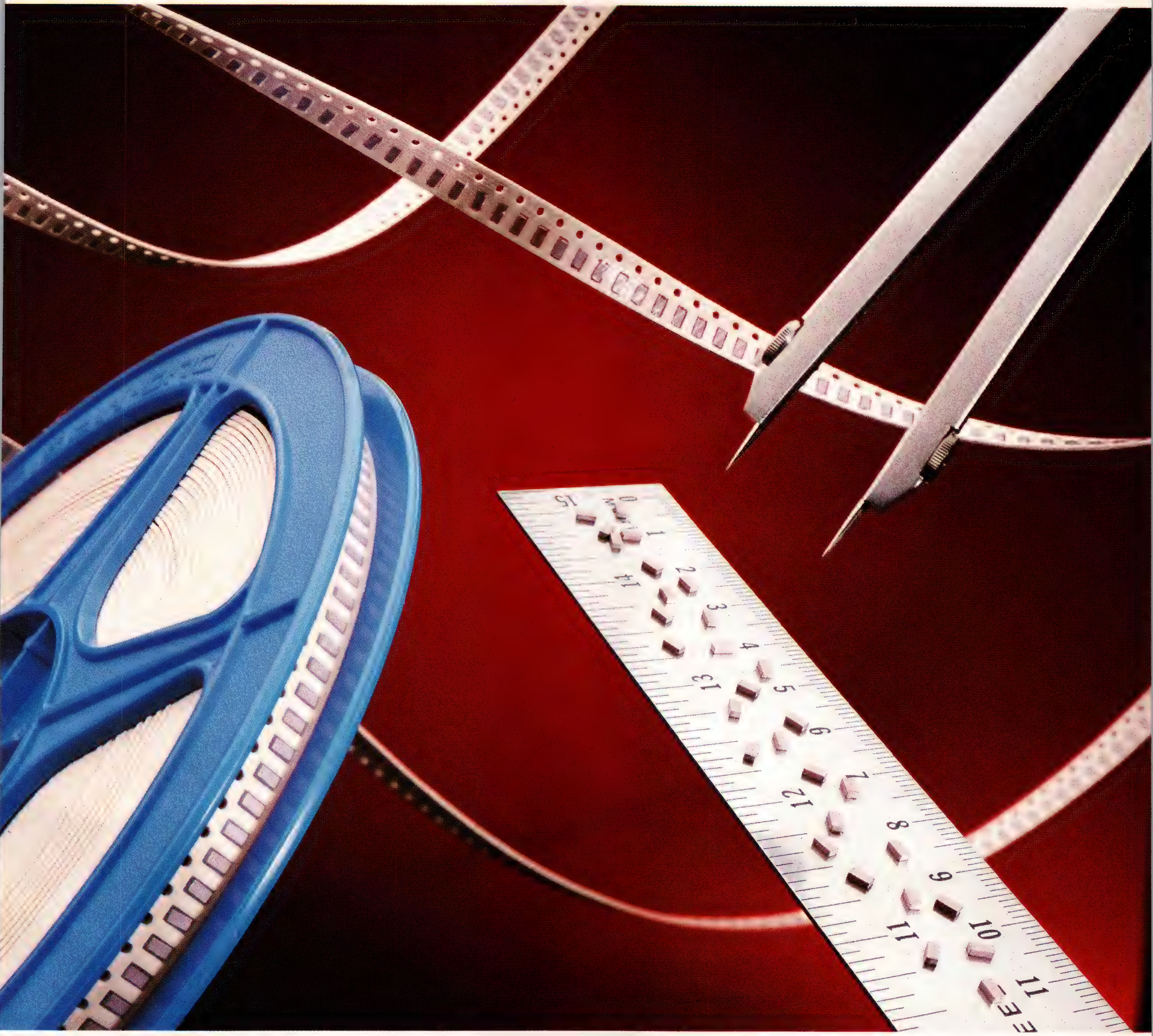

SPRAGUE CHIP CAPACITORS FIT EXACTING NEEDS.

Sprague Type 11C Monolythic® Ceramic Chip Capacitors are cost competitive and available today on 8mm reels for easy automatic placement and attachment to printed wiring boards and hybrid circuits. These multilayer chip capacitors are supplied with a choice of metallized terminations to fit the needs of both surface-mounting and hybrid technologies. They are furnished in a full range of capacitance and temperature characteristics. *Sprague Electric Company, a Penn Central unit,* Worldwide Hdqtrs., Lexington, MA. Write for Engineering Bulletin 6200F to Technical Literature Service, Sprague Electric Company, 41 Hampden Road, Mansfield, MA 02048-1807.

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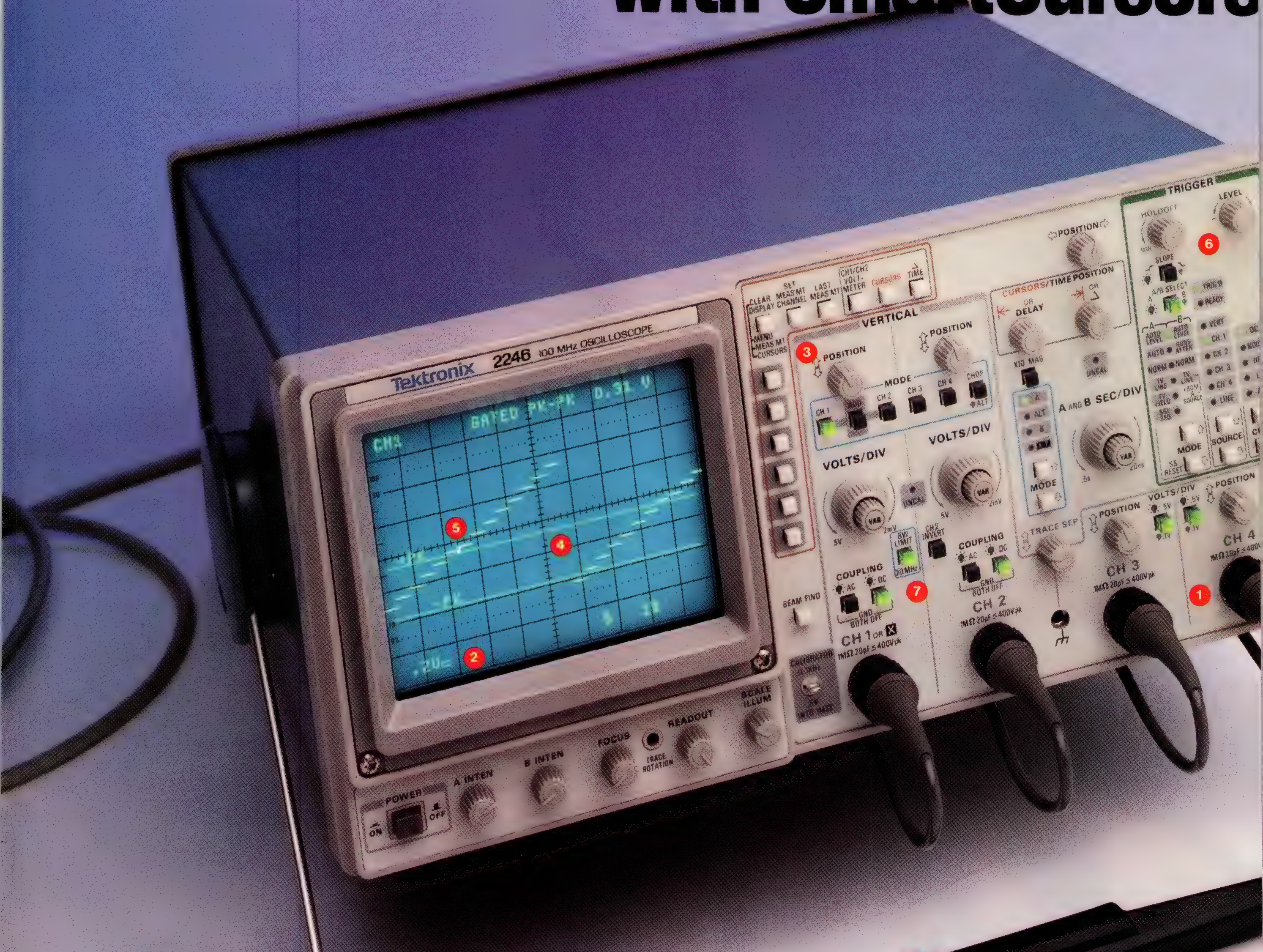
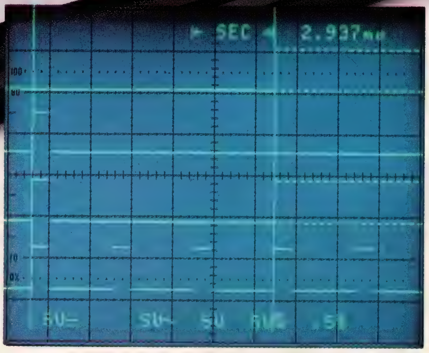
CIRCLE NO 125

New GPS Series with SmartCursors



①Four channels with 100 MHz bandwidth. ②CRT readout of scale factors and measurement results. ③Menu functions controlled by the top row of push buttons. ④SmartCursors™ track ± peak or peak-to-peak voltage measurements. ⑤Gated voltage mode makes it possible to itensify a portion of a waveform and make voltage measurements on that segment only. ⑥Versatile triggering lets you trigger the main or delayed sweep on any of the four channels. ⑦Backlit control buttons verify that a function is active.



The 2246 provides direct time readout information when seconds is selected in cursor mode. You also have 1/seconds in Hz and phase capability.

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ek sets the pace nd push-button ease.

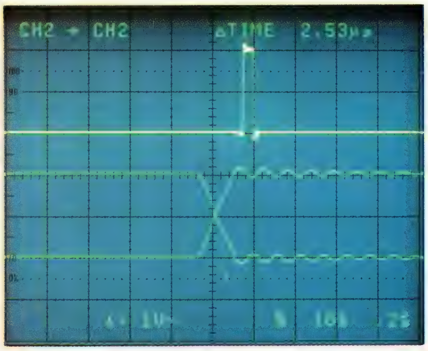
Work faster, smarter, with two new general purpose scopes from Tek. The four-channel, 100 MHz 2246 and 2245 set the new, fast pace for measurements made daily at the bench or in the field. They're easy to use and afford, by design. And backed by Tek's three-year warranty that includes the CRT.

On top: the 2246 with exclusive integrated push-button measurements. Your measurements are accessed through easy, pop-up menus and implemented at the touch of a button. Measure ± peak volts, peak-to-peak, dc volts and gated volts with new hands-off convenience and on-screen readout of values.

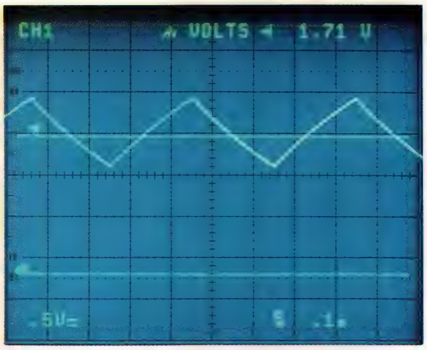
SmartCursors™ track voltmeter measurements in the 2246 and visually indicate where ground and trigger levels are located. Or use cursors in the manual mode for immediate, effortless measurement of waveform parameters like voltage, time, frequency, and phase.

Both scopes build on performance you haven't seen at the bandwidth or prices. Lab grade features include sweep speeds to 2 ns/div. Vertical sensitivity of 2 mV/div at full bandwidth for low-level signal capture. Plus trigger sensitivity to 0.25 div at 50 MHz, to 0.5 div at 150 MHz.

Features	2246	2245
Bandwidth	100 MHz	100 MHz
No. of Channels	4	4
Scale Factor Readout	Yes	Yes
SmartCursors™	Yes	No
Volts Cursors	Yes	No
Time Cursors	Yes	No
Voltmeter	Yes	No
Vertical Sensitivity	2 mV/div	2 mV/div
Max. Sweep Speed	2 ns/div	2 ns/div
Accuracy: Vert/Hor	2%/2%	2%/2%
Trigger Modes	Auto Level, Auto, Norm, TV Field, TV Line, Single Sweep	
Trigger Level Readout	Yes	No
Weight	16.5 lb/7.5 kg	16.5 lb/7.5 kg
Warranty	3-year on parts and labor including the CRT	
Price	$2400	$1875



Conventional ΔTime measurement is also available from the menu in the 2246 for increased timing accuracy. Shown above: a ΔTime measurement of pulse width.



The 2246 also makes it possible to measure either ΔVolts or absolute volts from ground.

Best of all, high performance comes with unmatched convenience. You can see it and feel it—in the responsive controls and simple front-panel design, in extensive on-screen scale factor readouts, and in simplified trigger operation that includes Tek's Auto Level mode for automatic triggering on any signal. Start to finish, the GPS Series saves steps and simplifies tasks.

Get out in front! Call toll-free today to order, to get more details or a videotape demonstration.
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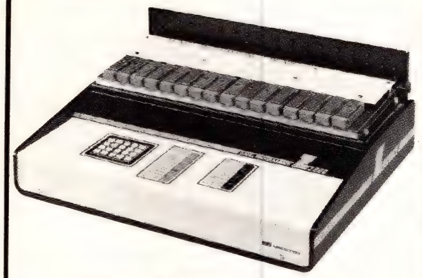
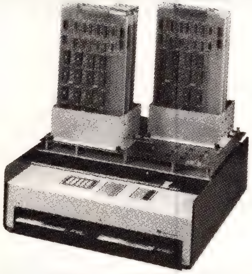
CIRCLE NO 126

AMERICA'S BEST PROGRAMMERS



Z-3000 HIGH VOLUME GANG/SET PROGRAMMER

- 14,000 27256s programmed per day.
- 32 EPROMs simultaneously with 1 to 8 DATA BLOCKS.
- 16 Intel or Motorola MCUs at a time.
- 64K to 256K bytes of DATA RAM.
- Simple one key programming operation.
- Two RS-232 ports with data transfer formats included.



Z-2500B IN-CIRCUIT MEMORY CARD PROGRAMMER

- Programs up to 32 memory cards with EPROMs or microcomputers at a time.
- Two 1.2 Mbyte DSDD floppy disk drives. Optional 20 Mbyte hard disk.
- Turnkey systems include programmer, terminal, custom interface hardware and software.
- Simple menu driven operation.

Z-1000B UNIVERSAL PROGRAMMER

- Over 600 PLDs, EPROMs, EEPROMs, bipolar PROMs and INTEL MCUs.
- Upgradeable PROM based software.
- Stand alone or PC/XT/AT operation.
- Two independent RS-232 ports.
- 64K or 256K bytes of DATA RAM.
- EXATRON handler interface is standard.

Z-1200B TWELVE SOCKET GANG/SET PROGRAMMER

- 2716-27512, 1 to 4 DATA BLOCKS.
- 64K to 256K bytes of DATA RAM.
- Software personality. No plug-ins.

ZAP SERIES low cost programmers for EPROMs and single-chip MCUs.

Z-400 for bipolar PROMs and EPROMs.

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CIRCLE NO 13

10 article on social consciousness (pg 293) without being strongly swayed by his personal ideology.

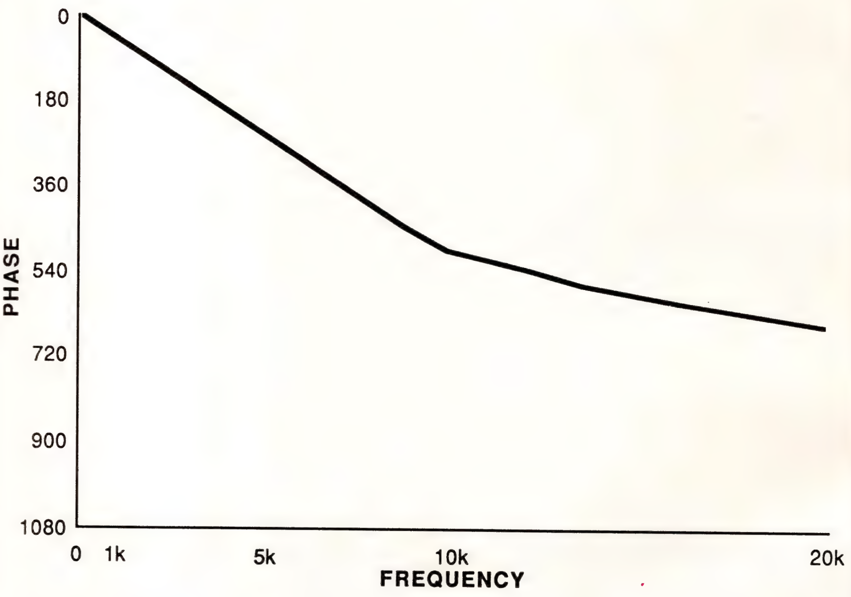
Thank you for providing a forum for this issue, which I believe deserves much thought.

Sincerely yours,
Jason Rusoff
Oakland, CA

Circuit's phase response isn't weird

Dear Editor:
Regarding Bill Travis's hands-on report "Low-cost PCs and software analyze analog circuits" (EDN, October 2, pg 163), I'd like to point out that the caption under Fig 7 (pg 168) is somewhat mistaken. The caption reads: "Excellent flatness, steep rolloff, and weird phase response characterize the filter in Fig 1. The sharp rolloff qualifies the filter as an excellent antialiasing circuit, but the bizarre phase response disqualifies it for applications needing good phase linearity."

In fact, the circuit's phase response is very linear. Because the inverse tangent routines return an angle between +180 and −180°, a foldover is occurring in the plot. The true phase response is more like that in the accompanying graph.



Sincerely yours,
Kevin McLaughlin
Senior Electrical Engineer
Motorola Inc
Boyton Beach, FL

(Ed Note: Mr McLaughlin is right. We stand corrected.)

DSP chips have 16-bit I/O ports

Dear Editor:
I would like to correct some errors regarding the Philips/Signetics PCB5010/11 DSP chips mentioned in Table 1 of Jon Titus's Special Report on DSP ICs (EDN, October 16, pg 162). The 5010 and 5011 can address 64k×16 bits of external data memory. The 5010 has one 16-bit I/O port; the 5011 has two. Both devices have four serial ports, two for input and two for output.

Sincerely yours,
Alex Goldberger
Signetics
Sunnyvale, CA

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The Tek 11000 Series is nothing less than a new generation of oscilloscopes. What you can do with it, and the way you work with it, will fundamentally alter your expectations of a scope.

These fully programmable scopes display more traces (up to 8) at higher bandwidths (up to 1 GHz), with greater accuracy (1% vertical) and include more new functions for expediting the capture and processing of data than can ever be listed here.

Two digitizing scopes exert the power of three 16-bit processors towards longer records, more powerful triggering and higher throughput than ever before. Two analog scopes virtually eliminate manual computation, even for the most complex measurements.

Most startling is the simplification and automation of the whole measurement and analysis process. Large displays, touch-screen control, pop-up menus and built-in intelligence unclutter the front panel and keep eyes focused on the display. For the first time, you need know nothing about a scope's technology to get the most out of it.

The 11000 Series continues the plug-in versatility of the Tek 7000 Series. Five new plug-ins and three new probes tailor 11000 Series scopes to a full range of applications, from design and debug to production test.

DIGITIZING	11401	11402	ANALOG	11301	11302
Bandwidth	500 MHz	1 GHz	Bandwidth	400 MHz	500 MHz
Risetime	700 ps	350 ps	Risetime	875 ps	700 ps
No. Channels[1]	1-12	1-12	No. Channels[1]	1-8	1-8
Vert. Sensitivity[4]	1 mV/div	1mV/div	Vert. Sensitivity[4]	1 mV/div	1 mV/div
Vert. Resolution	10-14 bits[3]	10-14 bits[3]			
Automatic Measurements	Min, Max, Mid, Mean, RMS, Peak-Peak, Rise, Fall, Width, Delay1, Cross, Period, Frequency, Main → Window Trigger, YT Area, YT Energy, Cursors		Automatic Measurements	Peak-Peak, Min, Max, Mid, Frequency, Period, Width, Duty Cycle	
Timebase Accuracy	100 ps + .002% of the measured interval		Built-in counter/timer	500 MHz 6 Function 10 digits	500 MHz 6 Function 10 digits

Demonstrations are now in progress throughout North America. To get in touch with the future of measurement, contact your local Tek sales engineer or call Tektronix at 1-800-547-1512.

---

[1] Up to 8 traces may be displayed at once from any of up to 12 input channels.
[2] Absolute DC accuracy with full scale offset or Vc.
[3] 14-bit resolution obtained using signal averaging.
[4] Except with 11A71 which has 10mV/div

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How the new echnology will simplify your life.

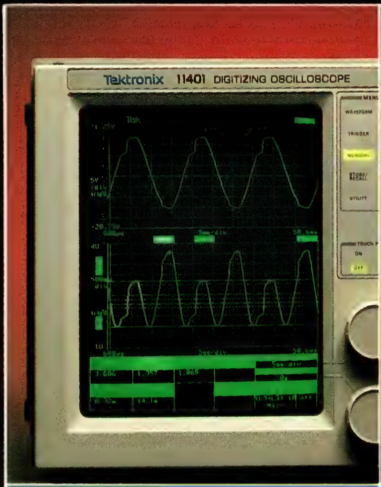
The 11000 Series, nakes it unnecessary o learn oscilloscope neory. You get more ut of your scope with ess effort than ever efore.

Mechanical front-anel controls have ll but vanished in avor of a touch-creen interface that resents only valid elections in logical roups. Select a ace, a trigger, a neasurement or ther function just by ouching the appro-riate area of the creen or by select-ng from pop-up nenus that fold lown out of the way nce selections are nade.

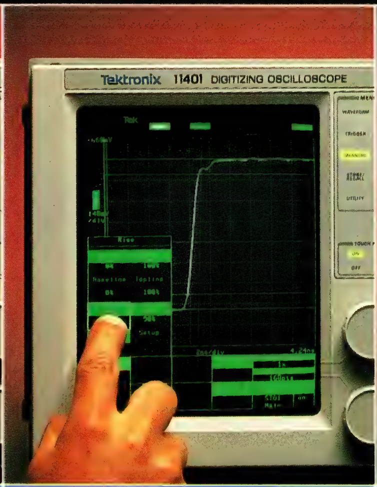
Or, push a button n the new probes o initiate an auto-ange or a sequence f stored test setups—your hands and eyes never eave the job.

11401/11402 Digitizing Oscilloscopes

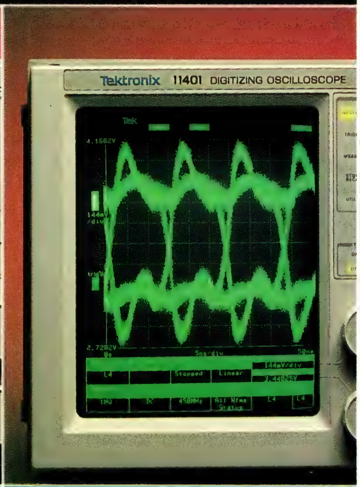
One example of innumerable waveform processing capabilities: square a voltage waveform and divide by a load resistance — (L3*L3)/10 — to make a power measurement.



Customize automatic measurements to meet your needs. Touching any measurement result, for example, causes annotation to appear showing exactly where the measurement is being taken.

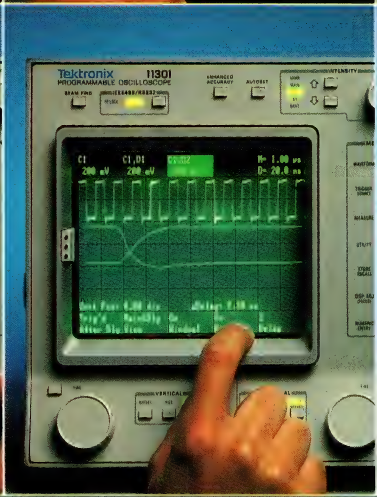


Point Accumulate Mode keeps all digitized points in display memory to help you handle complex displays such as eye diagrams, measure worst case jitter, or catch low rep-rate glitches.

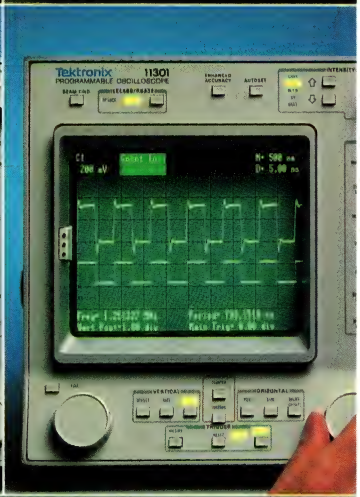


11301/11302 Analog Oscilloscopes

Call up cursors to help you make high-accuracy measurements, displayed in decibels, percent, degrees, volts or seconds.

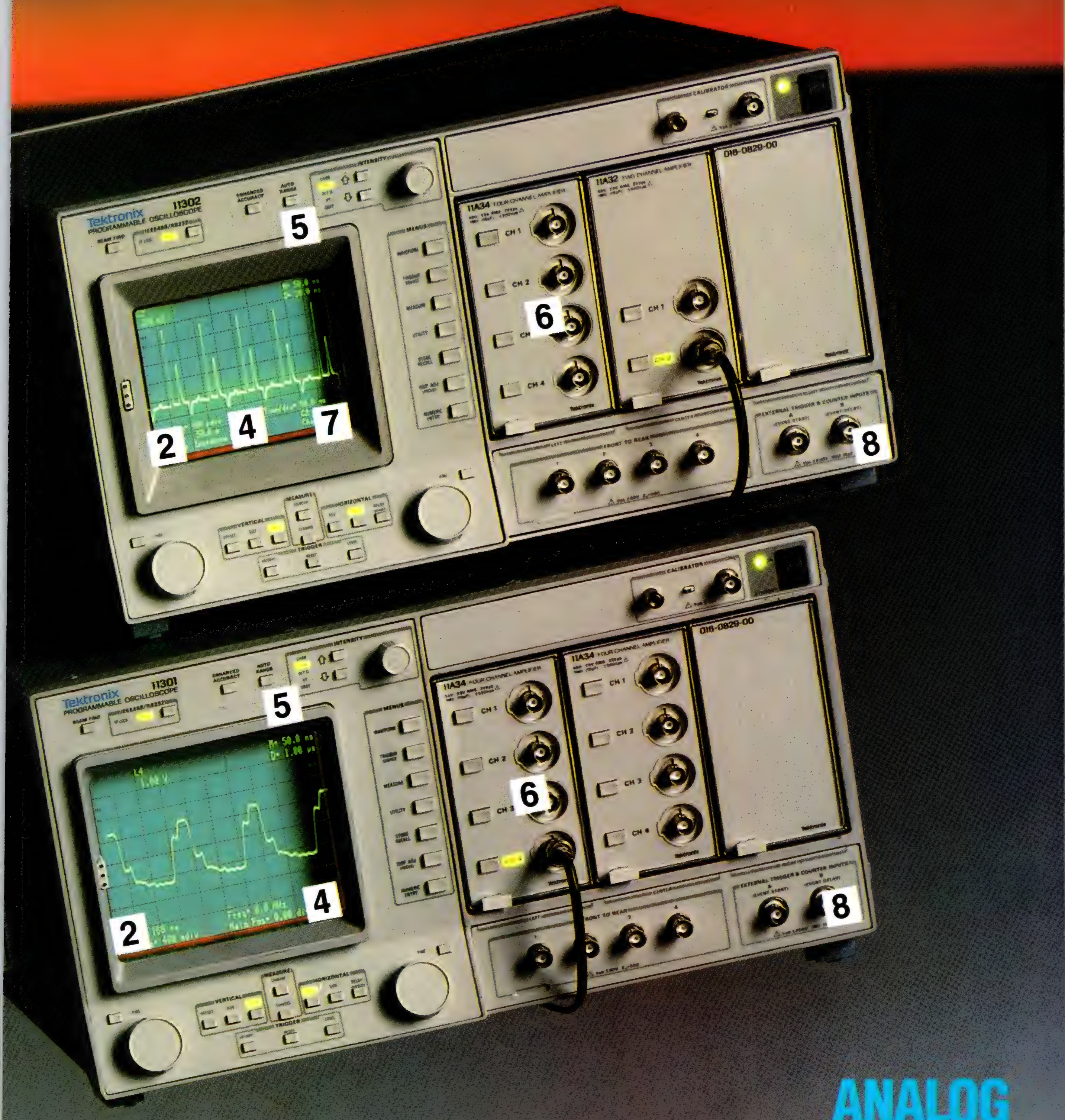


Dual delayed sweeps allow expansion of the main sweep for close examination and accurate measurement of waveform parameters such as risetime and falltime.



Integrated 500 MHz universal counter/timer includes a unique counter-view feature that lets you see exactly what the counter/timer is triggering on.

CIRCLE NO 40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PROGRAMMABLE OSCILLOSCOPE
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11301
11A34 FOUR CHANNEL AMPLIFIER
11A32 TWO CHANNEL AMPLIFIER
CALIBRATOR
CH 1
CH 2
CH 3
CH 4
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2
4
5
6
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5 AUTOSET FROM PROBE TIP. Push a button on the front panel or on the probe to set up a scaled and triggered waveform display, or to sequence automatically through a series of tests.

6 1 mV/DIV VERTICAL SENSITIVITY. Applies across the full bandwidth, right at the probe tip. Achievable on three new plug-ins.

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8 500 MHz SIX FUNCTION COUNTER/ TIMER. With 2 ns single shot resolution — 10 ps with averaging. Use with dual delayed sweeps for precise timing measurements between selected points. Counter/timer view trace ends guesswork.

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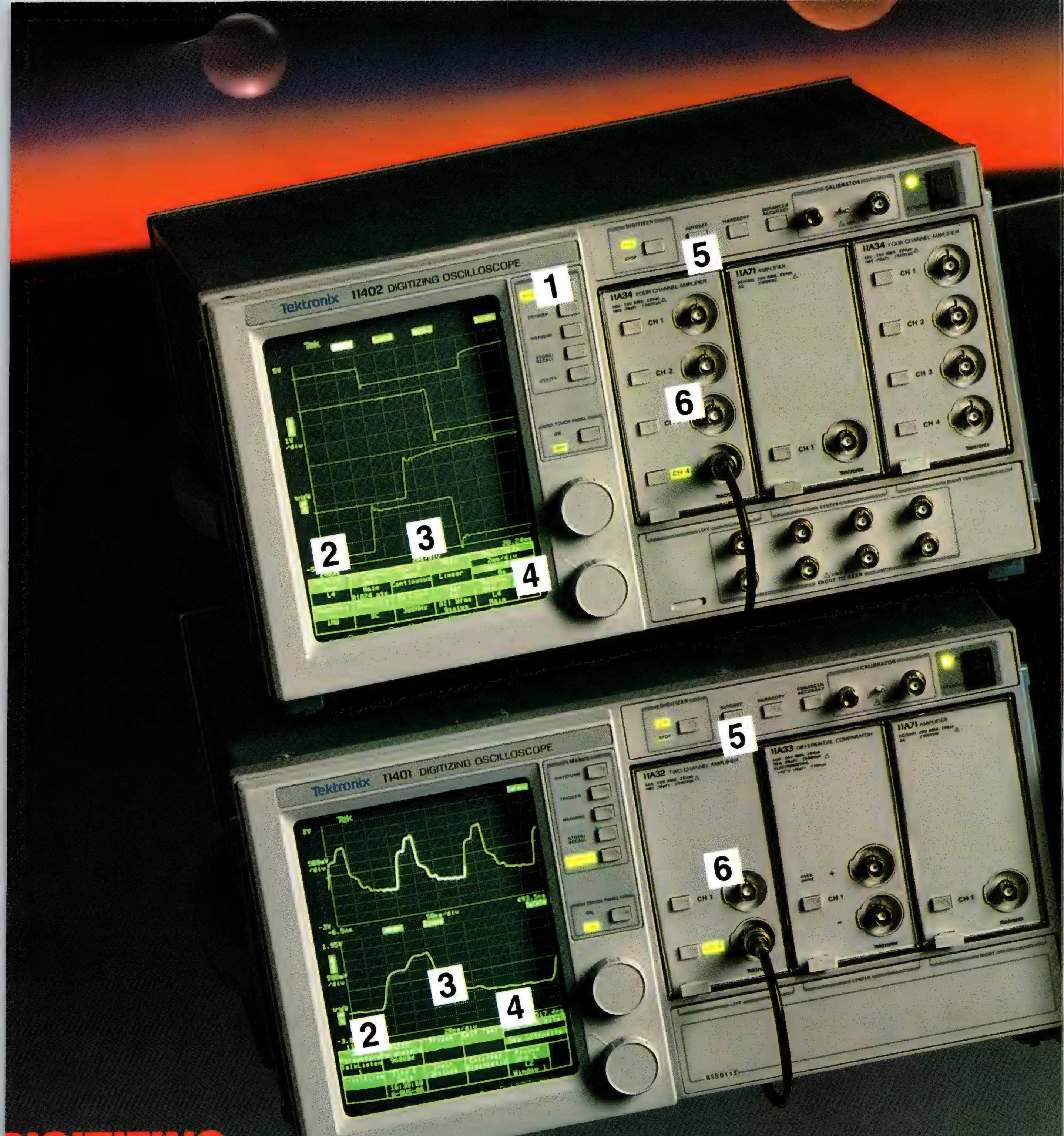
Tektronix 11402 DIGITIZING OSCILLOSCOPE
Tektronix 11401 DIGITIZING OSCILLOSCOPE
11A34 FOUR CHANNEL AMPLIFIER
11A71 AMPLIFIER
11A32 TWO CHANNEL AMPLIFIER
11A33 DIFFERENTIAL COMPARATOR
CALIBRATOR
1
2
3
4
5
6

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1 **1 GHz.** The 11402 Digitizing Oscilloscope fea- ures a full 1 GHz bandwidth ght at the probe tip—with no acrifice in vertical resolution —to help you make the most emanding voltage and timing easurements.

2 **UP TO 8 TRACES.** High-resolution screen lets you display up to eight waveforms simultaneously, with an update nearly as fast as an analog scope. No scopes ever let you see so much at once.

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A4

Our brains hav

The reliable side.

At Quantum, we put at least half our thinking into making disk drives reliable.

Our Q200 Series™ of 5¼″ intelligent disk drives is the perfect example of achieving near-perfection.

The specified mean time between failure for our Q200 Series is 25,000 operating hours. Our customers' incoming acceptance rate for all our products is over 99%. And the many ship-to-stock programs with our customers underscore a confidence level that's even higher.

The extraordinary reliability of our Q200 Series drives is the result of the out-of-the-ordinary things we do to make them that way.

Because we were the first to make intelligent 5¼″ disk drives, we have more field-proven experience in making them to last. And because we designed both the SCSI controller electronics and the drive, they truly perform as if they were made for each other.

The Q200 Series drives are available in 53MB, 80MB and 160MB (formatted) capacity models. And our new custom-designed, semi-automatic manufacturing line in Milpitas has the capacity to make these high quality drives at the rate of one every 30 seconds. So availability is one more thing you can rely on—from Quantum.

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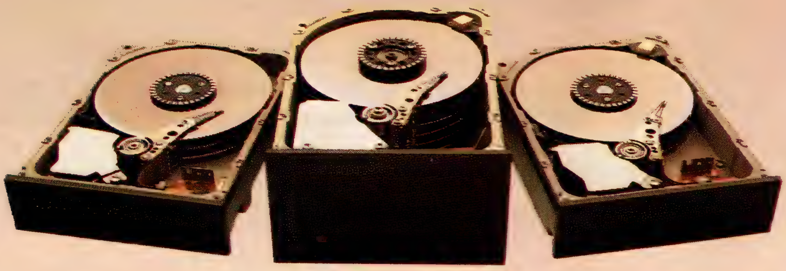

Q250 (53MB) **Q160 (160MB)** **Q280 (80MB)**

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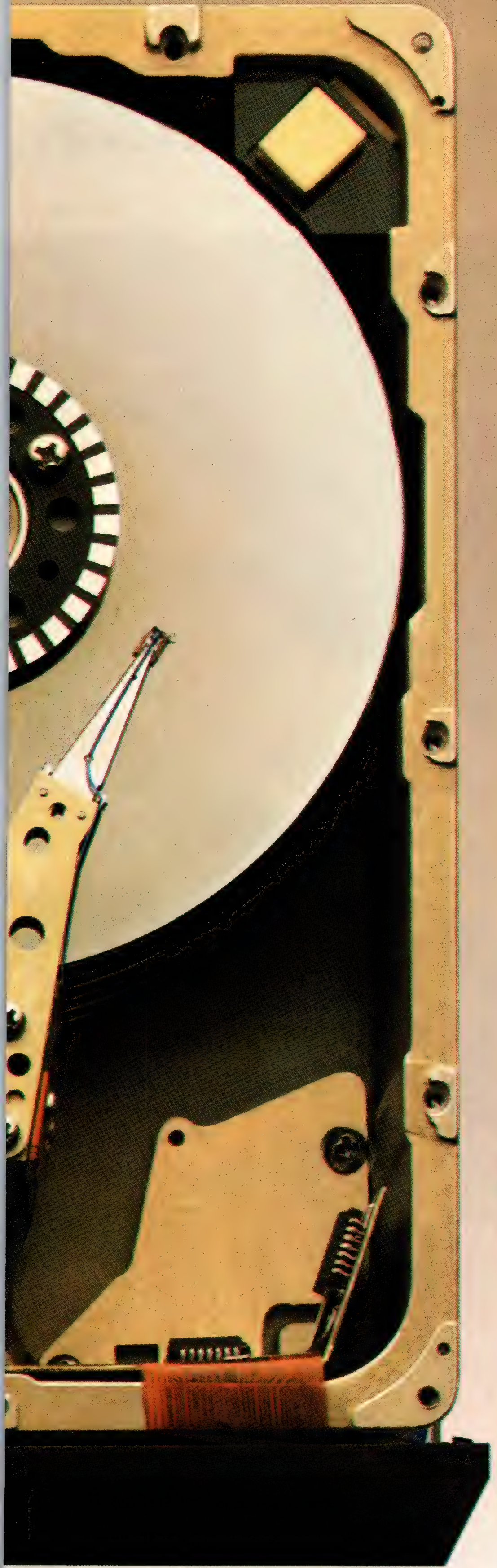
e two sides, too.



The innovative side.

At Quantum, we put at least half our thinking into making disk drives innovative.

Our Q200 Series™ of intelligent disk drives is the best example of doing things ever better.

The half-height 53MB and 80MB (formatted) capacity models were the very first intelligent drives introduced — a major advancement in disk drive architecture, integrating a custom SCSI controller into the drive itself.

Soon thereafter, we introduced our full-height 160MB (formatted) capacity intelligent disk drive. This new model in the Q200 family incorporates yet another major advance — DisCache,™ a look-ahead, high-speed memory to significantly increase data throughput, with programmable options for individual application needs.

All three models in the Q200 Series use the same heads, the same media, and the same integrated controller design. They also use the same SCSI interface and support the same software commands, utilizing the industry standard common command set. That's why we can guarantee compatibility among the family, making it easier than ever to upgrade and enhance your systems — now and with future products. So if you're looking for future innovations, Quantum is where to look first.

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Q250 (53MB) Q160 (160MB) Q280 (80MB)

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CIRCLE NO 84

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CIRCLE NO 85

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CIRCLE NO 15

CALENDAR

Annual Semicustom Circuits Conference, San Diego, CA. Mackintosh Consultants, 209 W Central St, Natick MA 01760. (617) 655-0001. Feb 18 to 20.

Nepcon West, Anaheim, CA. CEG, Box 5060, Des Plaines, IL 60017. (312) 299-9311. February 24 to 26.

ISSCC (International Solid-State Circuits Conference), New York, NY. Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. (305) 446-8193. February 25 to 27.

West Lightwave Expo, San Jose, CA. Lightwave, 235 Bear Hill Rd, Waltham, MA 02154. (617) 890-2700. February 25 to 27.

Spring National Design Engineering Show and Conference, Chicago, IL. CEG, 999 Summer St, Stamford, CT 06905. (203) 964-0000. March 2 to 5.

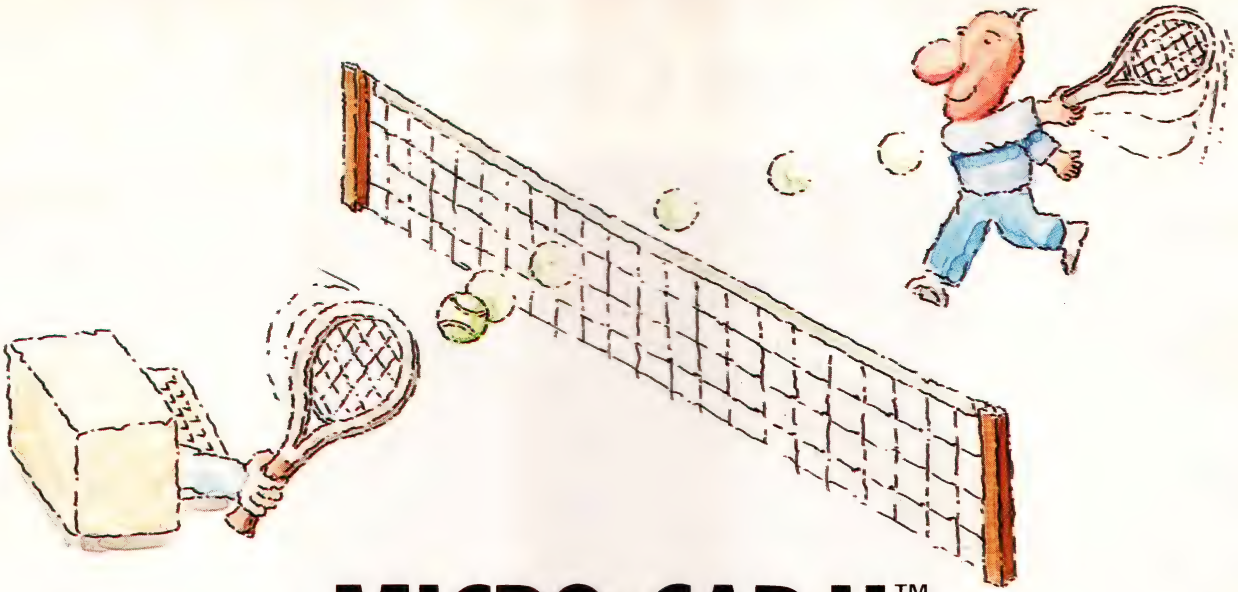
IEEE Applied Power Electronics Conference and Expo, San Diego, CA. Melissa Widerkehr, APEC '87, 655 15th St NW, Suite 300, Washington, DC 20005. (202) 347-5900. March 2 to 6.

Invitational Computer Conference, Austin, TX. B J Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. March 3.

Comdex in Japan, Tokyo, Japan. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. March 3 to 5.

Dexpo Europe (European DEC-Compatible Exhibition and Conference), London, UK. Expoconsul International, 3 Independence Way, Princeton, NJ 08540. (609) 987-9400. March 3 to 5.

Fourth Topical Meeting on Optical Data Storage, Lake Tahoe, NV. Optical Society of America, 1816 Jefferson Pl NW, Washington, DC



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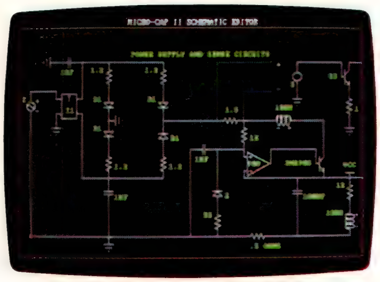

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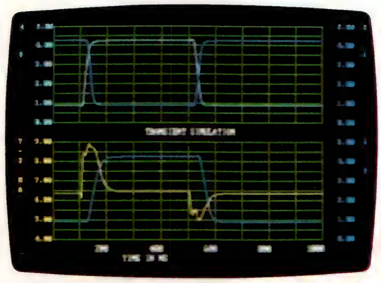

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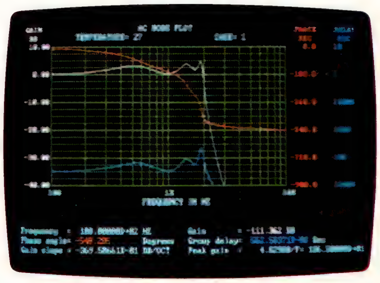

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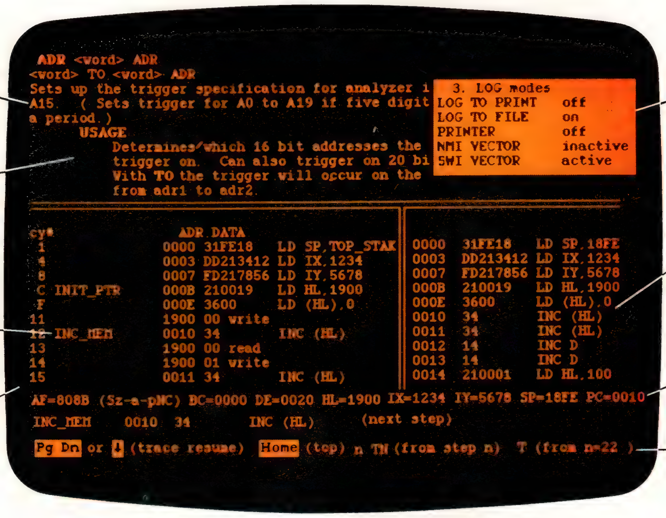
CIRCLE NO 86

Microprocessor Development Dreams Come True!



```
 ADR <word> ADR
<word> TO <word> ADR
Sets up the trigger specification for analyzer i   3. LOG modes
A15.  ( Sets trigger for A0 to A19 if five digit LOG TO PRINT    off
a period.)                                       LOG TO FILE     on
     USAGE                                       PRINTER         off
         Determines/which 16 bit addresses the   NMI VECTOR      inactive
         trigger on.  Can also trigger on 20 bi  SWI VECTOR      active
         With TO the trigger will occur on the
         from adr1 to adr2.

cy#                 ADR DATA
 1                 0000 31FE18   LD SP,TOP_STAK  0000  31FE18   LD SP,18FE
 4                 0003 DD213412 LD IX,1234      0003  DD213412 LD IX,1234
 8                 0007 FD217856 LD IY,5678      0007  FD217856 LD IY,5678
 C INIT_PTR        000B 210019   LD HL,1900      000B  210019   LD HL,1900
 F                 000E 3600     LD (HL),0       000E  3600     LD (HL),0
11                 1900 00 write                 0010  34       INC (HL)
12 INC_MEM         0010 34       INC (HL)        0011  34       INC (HL)
13                 1900 00 read                  0012  14       INC D
14                 1900 01 write                 0013  14       INC D
15                 0011 34       INC (HL)        0014  210001   LD HL,100
AF=808B (Sz-a-pNC) BC=0000 DE=0020 HL=1900 IX=1234 IY=5678 SP=18FE PC=0010
INC_MEM    0010  34        INC (HL)        (next step)
Pg Dn or ↓ (trace resume)  Home (top) n TN (from step n)  T (from n=22 )
```

On-Line Help menus,
Command Glossary,
and Word List.

Windows can be used
to view source files,
previous traces,
and more.

Symbol translation
or source code
line display.

Screen displays scroll off
into history buffer –
can be viewed later.

Pop-up Mode
Selection panel
called by soft key.

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in memory can be
compared with trace in
adjacent window.

Symbolic debug
register display.

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prompt line.

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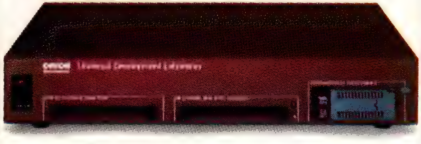

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An Integrated Software Environment, too!

Imagine being able to split your screen and look at real-time program traces and the source code that produced them at the same time! Then go to the On-Line Help or pop-up Mode Panels instantly.

If you see something on a trace that doesn't look like last time, you can hold it in one window while you scroll back through your previous displays.

If you set a breakpoint and single-step, you can then go back to using the analyzer without missing a beat. You can even execute a DOS batch file from UniLab to edit, assemble, and link, then automatically load the new program and symbol table. UniLab uses the full power of the PC.

Find bugs fast with Hardware-assisted Debugging

The traditional way to look for bugs is to single-step through suspect parts of the code until you catch it in the act. This requires a lot of guessing and wasting time.

With UniLab's built-in analyzer, you eliminate the guesswork. Just describe the bug symptom as a trigger, and let the UniLab hardware search for it as your program runs in real time. UniLab will show you a trace of the program steps leading up to the symptom, almost like magic.

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CIRCLE NO 87

CALENDAR

20036. (202) 223-0920. March 11 to 13.

Design and Manufacture of Surface Mount Technology (symposium), Longmont, CO. New Technologies and Design, Box 376, Longmont, CO 80502. (303) 651-2535. March 12 to 13.

Northeast Bioengineering Conference, Philadelphia, PA. IEEE, 6411 Chillum Pl NW, Washington, DC 20012. (202) 785-0017. March 12 to 13.

Modern Electronic Packaging, Torrance, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. March 16 to 18.

International Military Fiber Optic and Communications Exposition, Washington, DC. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (617) 232-3111. March 16 to 19.

CIM in Practice—Company Experiences, Seattle, WA. Society of Manufacturing Engineers, Computer and Automated Systems Association, Greater Seattle Chapter #282, Box 1445, Renton, WA 98057. March 17 to 18.

Computer Graphics '87, Philadelphia, PA. National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031. (703) 698-9600. March 22 to 26.

Fundamentals of Failure Analysis (seminar), Chicago, IL. L J Broutman & Associates, 3424 S State St, Chicago, IL 60616. (312) 842-4100. March 23 to 25.

IEEE VLSI Test Workshop, Atlantic City, NJ. Wesley Radcliffe, IBM, East Fishkill Facility, Bldg 321-5E1, Dept 277, Hopewell Junction, NY 12533. (914) 894-4346. March 24 to 25.

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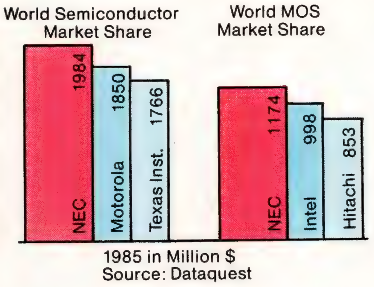

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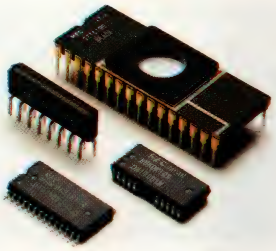

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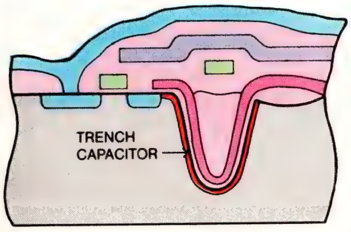

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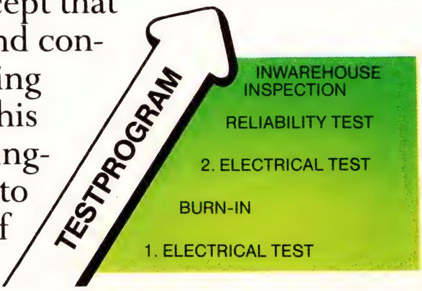

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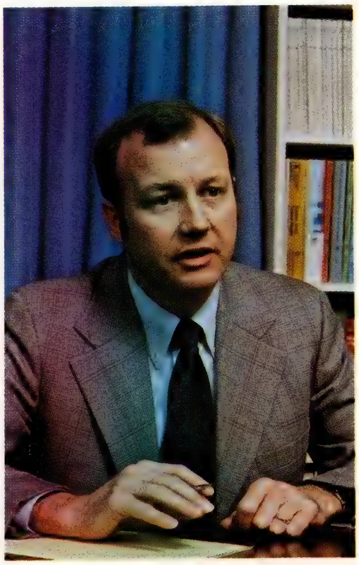
CIRCLE NO 53

EDITORIAL

Keep your eye on the doughnut



My dad used to say, "Keep your eye upon the doughnut and not upon the hole." Unfortunately, it is very easy to lose sight of goals and focus attention elsewhere. Many designs and businesses go astray because people set goals poorly or forget them all together.

For example, the people who designed my wife's blender forgot their goal was to build an appliance that chops food into little bits or mixes ingredients. Instead, they produced a technical marvel that has rows of buttons with vague legends such as "whip," "blend," and "puree." When we want to mix things, we pull out the egg beater. There's no doubt about what it does, and we can adjust the speed easily. Likewise, the airlines forget they are in the transportation business. They think their job is flying planes from one airport to another. If they realized they were in the transportation business, they would take good care of baggage, help us get to the proper terminal quickly, and make the check-in process easy to endure.

Consider also the National Association of Homebuilders (NAHB), which works in concert with 41 manufacturers on the "Smarthouse" project. The participants want to wire new houses with special cables that distribute power and control signals to each outlet. The new outlets and wires will let you control appliances remotely, and they will let appliances send messages throughout your home. For example, the dishwasher might send a message to your TV set when the dishes are done.

In its haste to adopt new technologies, it seems the NAHB forgot a goal its members depend on to stay in business: affordable housing. In many areas, the cost of a new house is already very high. Consequently, most new-home buyers will balk at spending an extra $1000 to $2000 to control their microwave oven from the bathroom. Taking advantage of the new wiring requires new smart appliances, which add cost too.

When you start your next design project, set goals clearly, keep them in mind constantly, and review them regularly. It takes effort to keep yourself headed toward them, but it's worth it. If you're ever in doubt about how maintaining clear goals can keep you from straying too far, just remember the appliance, homebuilding, and airline industries.

Jon Titus

Jon Titus
Editor

16-Bit-Slice CMOS,

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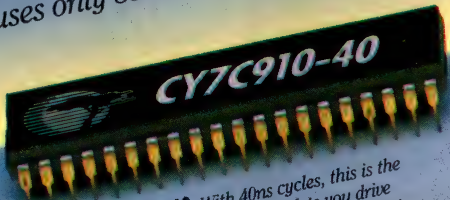

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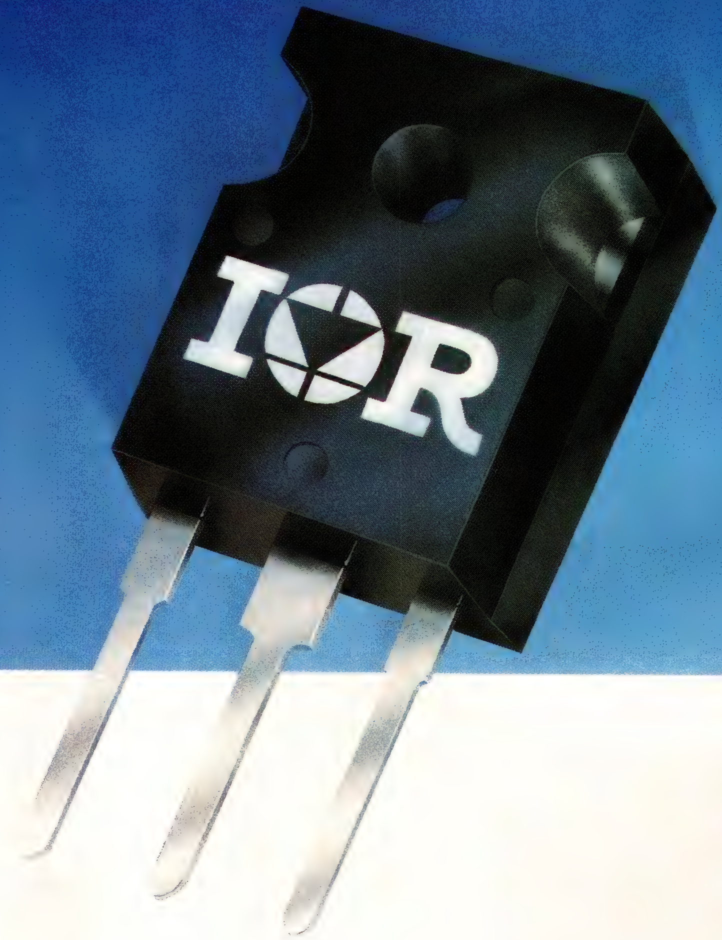

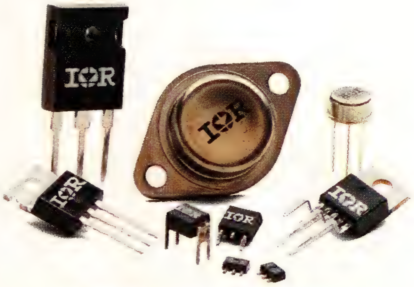

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CIRCLE NO 89

Project-management software for PCs helps you map out a plan for your project

Steven H Leibson,
Regional Editor

If you're responsible for managing a project from start to finish, you can use a personal computer and a software project-management package for activity planning, scheduling, and tracking. Project-management software is not only valuable in the day-to-day implementation of a project, it's also helpful in the planning stages. No matter whether you're working for your immediate boss, corporate management, or a customer, you can use a project-management program to generate a detailed plan and presentation package for the early stages of project proposals and funding.

Project-management software programs are no more project managers than word-processing programs are authors. They are merely specialized database tools that aid you in planning, scheduling, tracking, and controlling projects. Every project involves common objectives and resources. To achieve your objectives, you have to schedule and track the use of such resources as people, equipment, work space, and money.

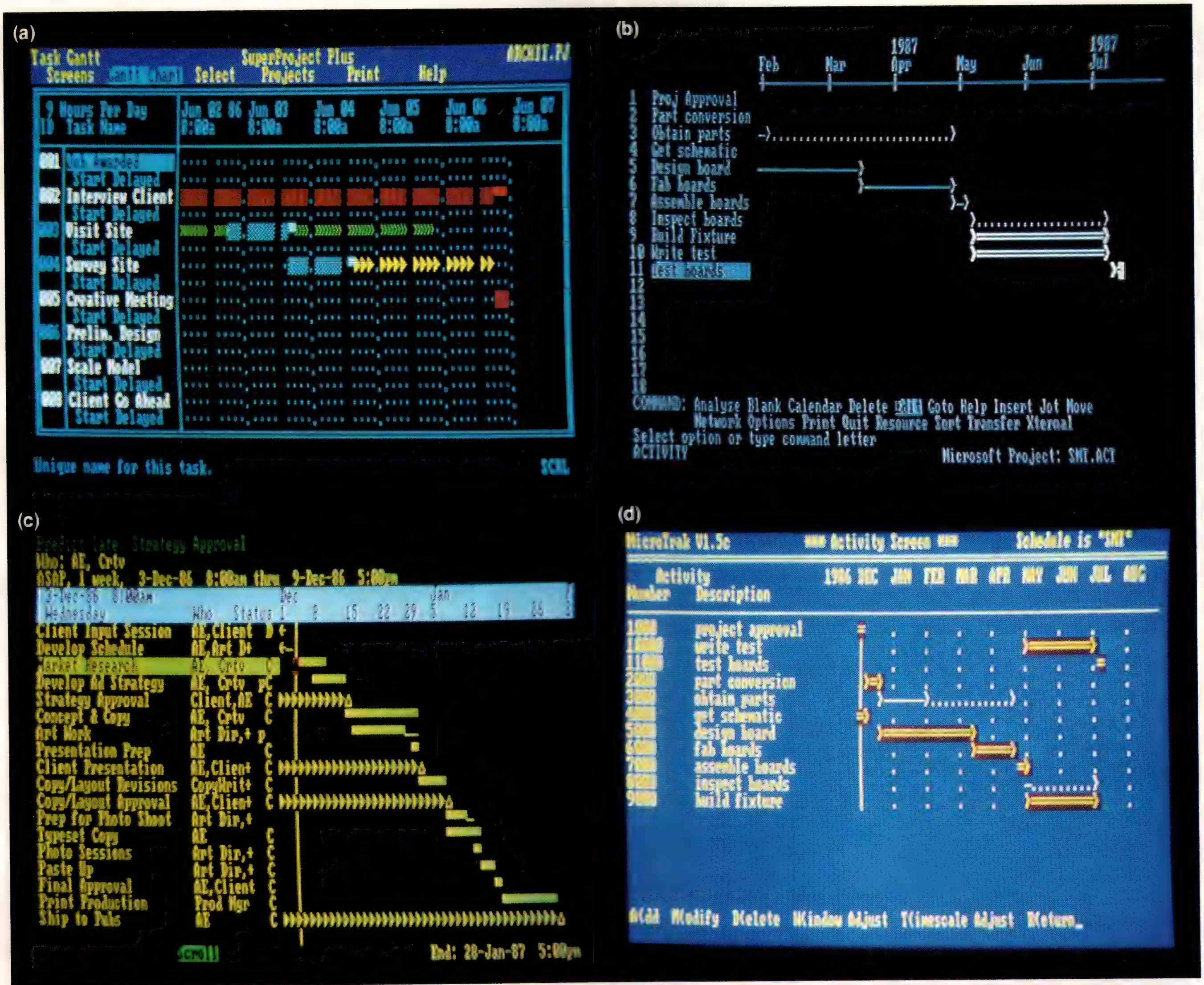
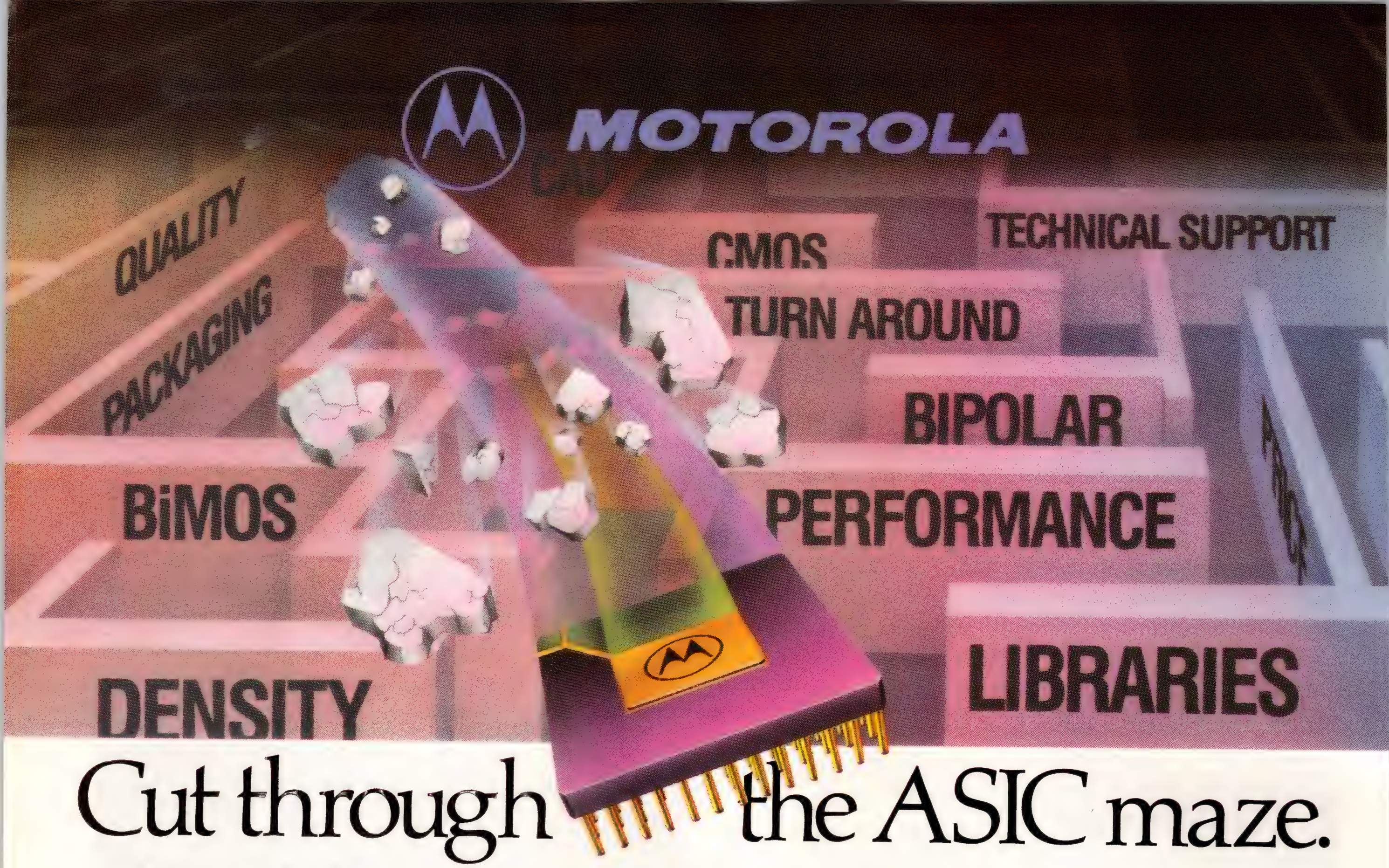


Fig 1—A Gantt chart plots project activities *against time. These screen shots present Gantt charts as rendered by Superproject Plus **(a)**, Microsoft Project **(b)**, Time Line **(c)**, and MicroTrak **(d)**.*



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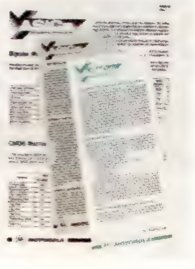

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You'll find dozens of programs to choose from. For this article, we've evaluated six representative project-management packages: Microsoft Project, Primavera Project Planner, Breakthrough Software's Time Line, Software Publishing's Harvard Total Project Manager, Computer Associates' Superproject Plus, and SofTrak Systems' MicroTrak. Although all six programs run on an IBM PC or compatible, they vary in cost, simplicity of use, and capability, which is true of all the project - management packages you'll encounter. We selected these products based on software reviews appearing in several magazines for users of IBM PC and compatible computers **(Refs 1, 2, 3, 4, 5, 6).**

In addition, we tried Individual Software's (Foster City, CA) *Individual Training for Project Management,* an interactive training disk. This product, which costs $69.95, introduces you to the basic concepts of project-management software without referring to any one particular program. It took about two hours to complete.

Most of the background material for this article came from this course and from two books: *Project Management Using Microcomputers* **(Ref 7),** and *Microcomputer Project Management Software Comparison Report* **(Ref 8).**

Shopping for a program

As a result of our experience with these project-management products, we strongly suggest you examine several project-management programs before purchasing one. Due to the complexities of managing a project, software project managers are intricate programs. Fortunately, all the products we tried included excellent tutorials; they require one to four hours to complete. If you can't find a computer store willing to let you sit down with a product for perhaps half a day, then you might want to try a low-cost demonstration version. Some vendors in **Table 1** offer such products.

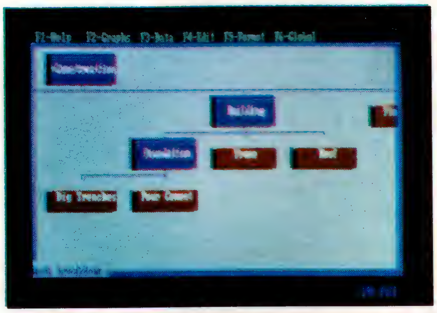

Fig 2—Harvard Total Project Manager, *a software package from Software Publishing, supports a WBS, a graphic method of designing a project from the top and working down.*

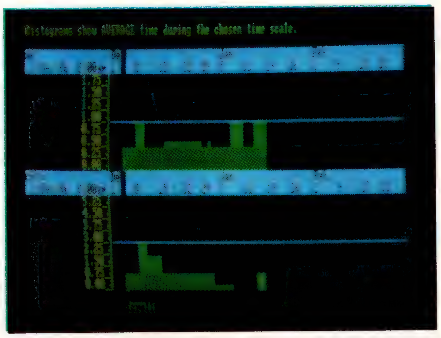

Fig 3—This 2-resource histogram, *part of the Time Line package, aids in resource leveling by graphically showing you time periods when resources are overallocated.*

Manual (pencil and paper) project-management techniques developed over the years serve as the models for today's project-management software programs. A Gantt bar chart, named for Henry Gantt, who developed it during World War I, plots the tasks to be done during a project against time, showing when each task is scheduled to start and (consequently) end. In addition, a Gantt chart shows what tasks are scheduled to be performed simultaneously and which thus might cause a resource-allocation conflict.

The most prevalent viewing model in project-management software is the Gantt chart **(Fig 1).** Of the products we tried, MicroTrak and Time Line both use the Gantt chart as the only point for entering project tasks. As you enter various project tasks, you see your project take shape on the displayed Gantt chart. The Time Line package includes extra information on its Gantt chart, telling you what resources are allocated to what tasks as well as the status of those tasks (done, critical, etc).

Outline a project with a WBS

It's not always easy to make a complete list of tasks at a project's conception, especially for large, complex projects. Another type of viewing model, a work breakdown structure (WBS), provides a simple technique for generating such a list of tasks. Essentially a graphic outline of the project, a WBS allows you to start at the top, creating your project from high-level objectives and working your way down.

You successively break the project components into smaller and smaller pieces until you reach the task level. These tasks then form the basis for the project's Gantt chart. Harvard Total Project Manager supports the WBS viewing model for entering and modifying a project **(Fig 2).**

Project management for Polaris

In the late 1950s, defense contractors, in conjunction with the US Navy Special Projects Office, developed the program evaluation and review technique (PERT) for the Polaris missile program. PERT attempts to deal with uncertain development times by using weighted averages of optimistic, pessimistic, and most-likely task-duration estimates.

At about the same time, DuPont and Remington Rand developed the critical-path method (CPM). CPM focuses attention on a project's most time-consuming sequence of tasks. Any delay in a task on the critical path delays the entire project. Tasks not on the critical path have a float or slack time, which may come in handy as unplanned events occur.

Both PERT and CPM, as originally conceived, use a precedence network diagram called an activity-on-the-arrow (AOA) network as the project-viewing model. This model shows tasks as arrows and events as nodes. Each task starts and ends at an event and is identified by the nodes at the task arrow's head and tail. This representation creates a problem because tasks that begin and end at the same event have nonunique names. To alleviate this problem, you must create "dummy" events so that each task ends at a different event and has a unique name.

A different network representation, developed in 1958 and called an activity-on-the-node (AON) network, circumvents this problem altogether. AON networks represent different tasks as different nodes, each with a unique name, and link those tasks with arrows showing how they are related.

Expand task relationships

Both AON and AOA networks support only one type of relationship between tasks: finish-to-start. In the idealistic world of AON- and AOA-network diagrams, one task must finish before its successor may start. In addition, both network representations assume that a task starts immediately after its predecessor finishes. The precedence diagram method (PDM), a refinement of AON representation, adds start-to-start and finish-to-finish relationships between nodes and allows for a delay factor (lag) between tasks.

If you manage projects that generally have simple relationships between tasks, software project managers that support AON networks may suffice for your application. Products that support PDM networks allow you to handle more-complex-activity relationships. Most of the project-management programs we tried support only AON or PDM networks, almost universally referring to these representations as PERT charts, although none of the six products supports PERT's uncertainty-of-task-duration feature.

Primavera Project Planner supports both AOA and PDM networks. Harvard Total Project Manager and SuperProject Plus allow you to edit your project from the network screen as well as from the Gantt screen. Other programs generate the network representation of the project as a report.

When selecting a project-management program, you should consider how many tasks you'll typically manage during a project. **Table 1** shows the maximum number of tasks each of the six project-management packages will accept given a host with 640k bytes of memory. Harvard Total Project Manager, Microsoft Project, Time Line, and SuperProject Plus accommodate subprojects that help you structure your plan into manageable pieces.

Subprojects also extend the maximum number of activities a project-management program can handle. Each subproject can have as many tasks as a project, even though the entire subproject represents only one task in the main project's network.

Assigning resources to tasks

As mentioned earlier, the completion of every task (and hence project) depends on the resources available. The two significant things about resources you must keep in mind when managing a project are that resources are finite and that they cost money to use. For instance, you may find certain resources overallocated during some time periods in your preliminary plan.

One way to overcome this problem involves resource leveling. Some products, including Microsoft Project, support only manual resource leveling. This leveling gives you the most control. To help in leveling resources, a resource histogram screen **(Fig 3)** aids in finding and resolving resource-allocation conflicts by graphically showing you when a resource is overallocated.

Several project managers offer the option of automatic resource leveling. Although SuperProject Plus supports manual leveling, it also levels resources automatically by delaying the starting dates of tasks with conflicting resource requirements. You must use automatic leveling with care because delaying those tasks on the critical path will postpone a project's completion date. Delaying noncritical tasks beyond their float time has a similar effect.

TABLE 1—REPRESENTATIVE PROJECT-MANAGEMENT SOFTWARE FOR IBM PCs AND COMPATIBLES

MANUFACTURER	PRODUCT	VERSION TESTED	PRICE	DEMO COST	TASKS/ PROJECT OR SUB-PROJECTS	GRAPHICS MODULE	GRAPHICS-MODULE COST
BREAKTHROUGH SOFTWARE	TIME LINE	2.00A	$495	$10	1000	TIME LINE GRAPHICS	$195
COMPUTER ASSOCIATES	SUPER-PROJECT PLUS	2.0	$495	SEE NOTE	999	INCLUDED	—
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All project-management programs produce tabular reports: lists of activities, data on individual activities, project costs, resource usage, and a host of others. Sorting and filtering features allow you to customize standard reports and extract only the information you want instead of subjecting yourself to a deluge of data. Finally, printed re-

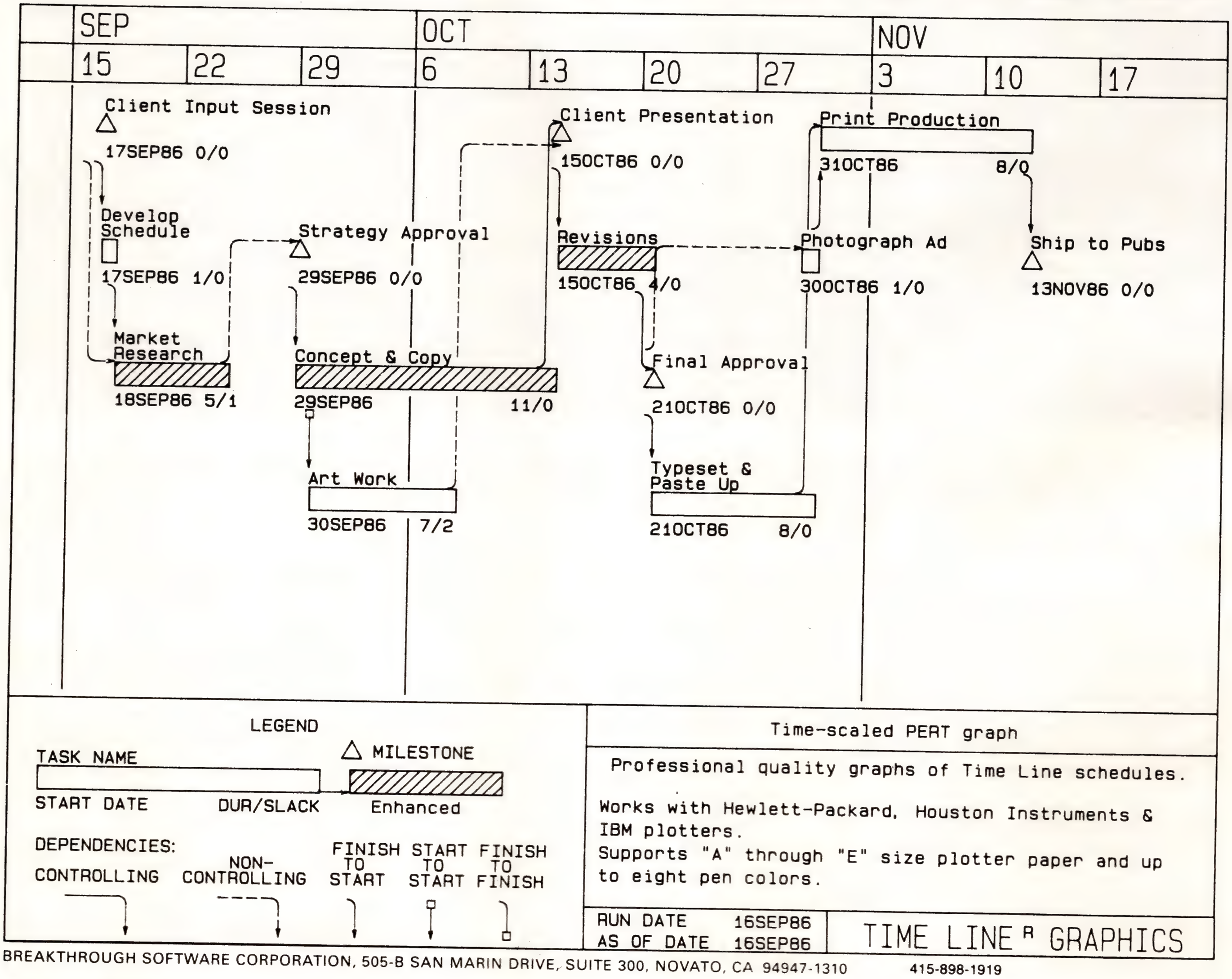
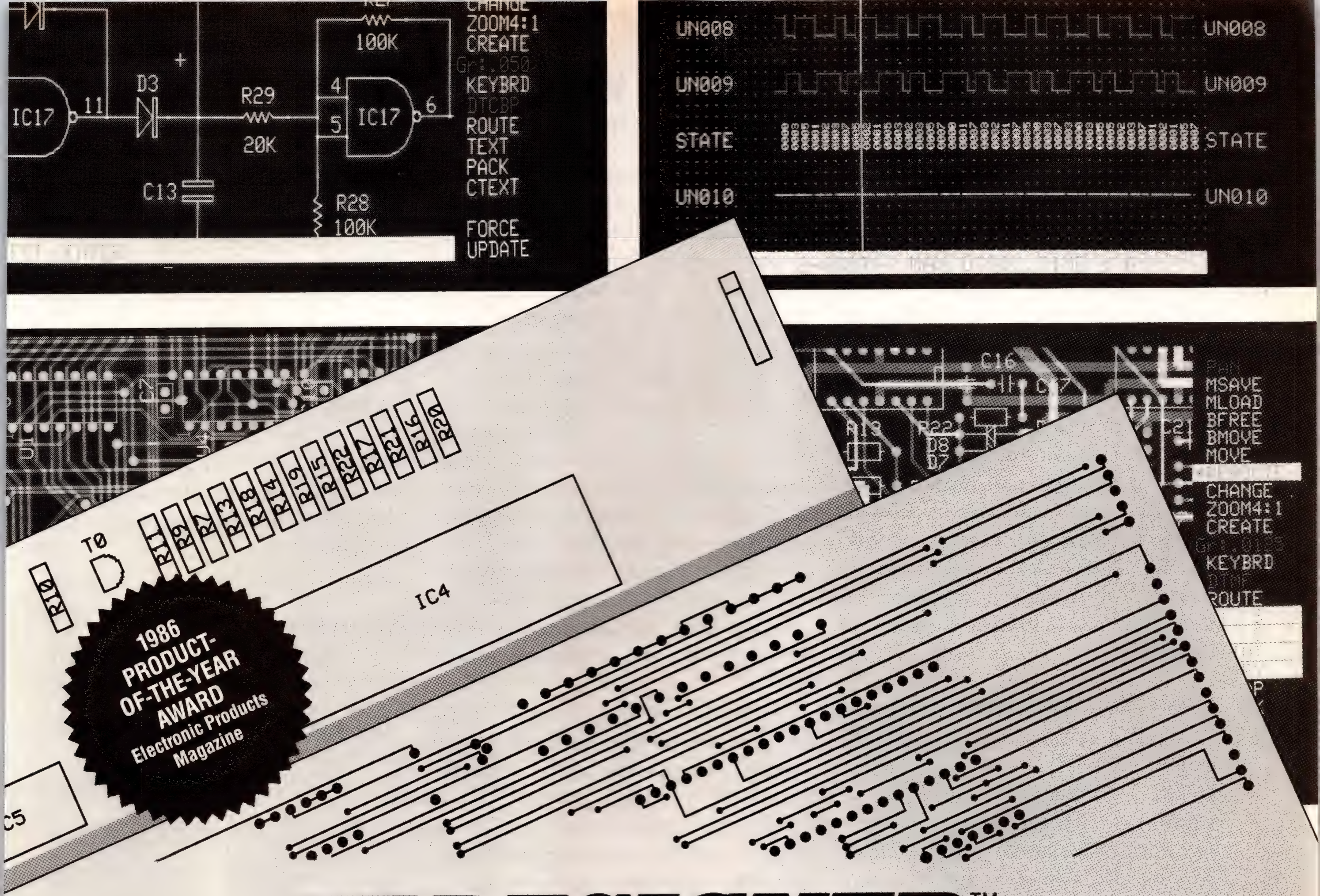


Fig 4—A plotted precedence network shows far more detail *than can be displayed on a CRT screen, as this Time Line plot shows.*



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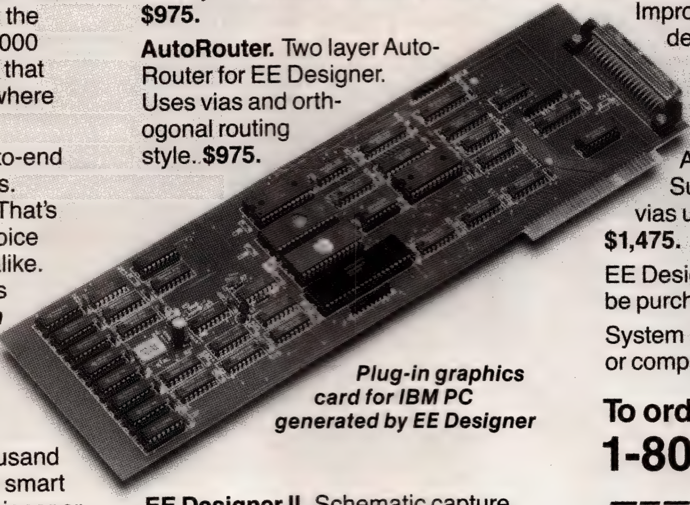

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ports not only tell you the status of your project, they allow you to show your clients that status as well.

Graphic reports give you a better view of your project's structure, as well as its progress towards completion, through network diagrams and Gantt charts **(Fig 4)**. Microsoft Project includes a graphic report generator and graphic driver for dot-matrix printers. Harvard Total Project Manager and SuperProject Plus can drive both printers and pen plotters. SofTrak Systems, Breakthrough Software, and Primavera Systems offer accessory graphic-report programs for their products **(Table 1)**.

Export data to other programs

Several project-management programs support import and export facilities, which allow you to move your project information to other software packages for further analysis or other processing. Popular export formats include Lotus 1-2-3, dBase II and III, and ASCII files.

Microsoft and Primavera Systems jointly offer a utility program that allows Microsoft Project users to pass project-schedule files to Primavera Project Planner and to Primavision, Primavera's graphic reporting package. Thus, a project manager using Primavera Project Planner can coordinate the projects of several other managers who are using Microsoft Project.

Once you've finalized your plan, you can use the detailed reports that the project-management software has produced to convince your client to go ahead with the project. As the project begins and progresses through the planned tasks, reality will inevitably rear its head and refuse to conform to your original Gantt chart. Resources won't be available when planned (people may become ill, equipment might break), extra tasks will become necessary, or your client may change his mind about the original objectives of the project.

Tracking a project through schedule changes is one of the tougher tasks a project-management package must perform. Ideally, as a project progresses you should be able to compare the original schedule (the baseline) with the latest revised schedule and with the project's current activity status. Not all packages offer these capabilities, though.

SuperProject Plus maintains planned (baseline), scheduled (current plan), and actual task-start and -finish dates. Harvard Total Project Manager maintains a baseline as part of each project file. Microsoft Project has a schedule-analyzer function that compares two different project files, allowing you to compare either the baseline plan against the current plan or the actual schedule against either plan. You can also save different Microsoft Project schedules during a project's implementation and compare any of these to the original baseline plan. Time Line has a similar feature allowing you to generate an actual-vs-planned report comparing two project schedules. **EDN**

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For more information . . .

For more information on the project-management software programs described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

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NEC	µPD70108/116 (V20/30)	DIP40P	○	
	µPD70208/216 (V40/50)	PGA	○	
MOTOROLA	MC68000	DIP64P,PGA68P		○

PROCESSOR (8bit)		PKG	SA2000
ZILOG	Z80CMOS (Z80, Z80A, Z80C)	DIP40P	○
	Z80H (Z80, Z80A, Z80B, Z80H)	DIP40P	○
	Z8 (Z8601/03/11/13-12R)	DIP40P	○
	SUPER-8 (Z8310-33)	DIP40/48P	○
INTEL	80C85, 8085AH-2	DIP40P	○
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MITSUBISHI	M50734SP	SDIP64P	○
	M50745	SDIP64P	○
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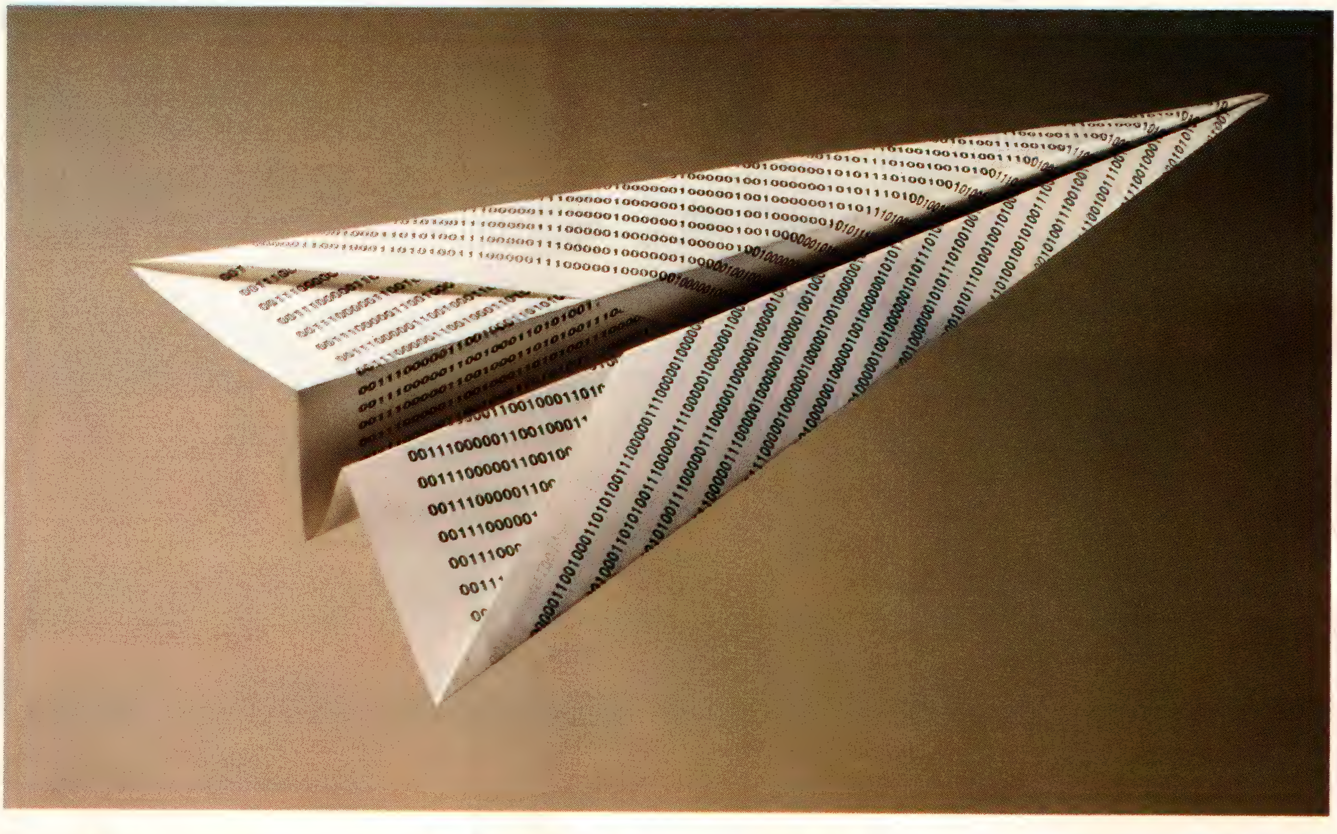

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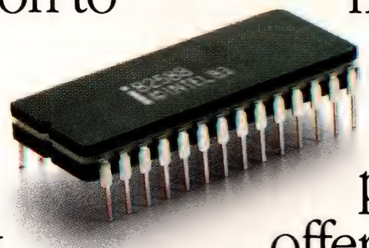

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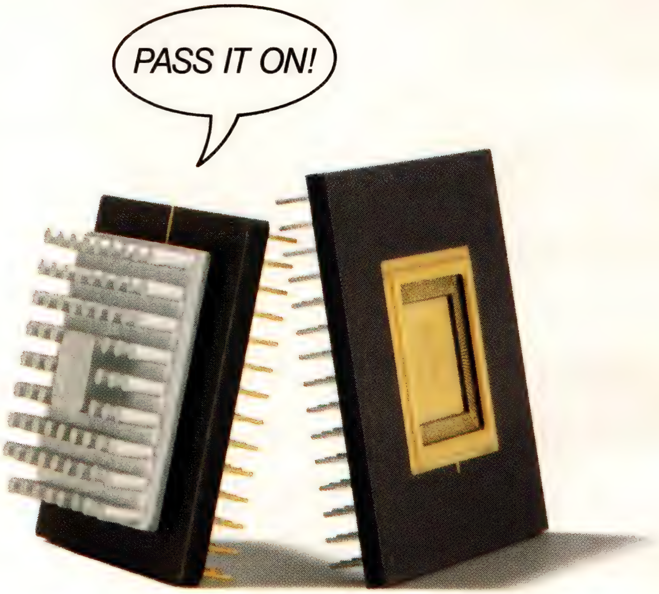

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CIRCLE NO 93

Bit-error-rate testers troubleshoot data links in real time

Peter Harold, *European Editor*

When you're networking data over a wide-area network—such as a public switched telephone network (PSTN), leased phone lines, or a packet-switching network—it's important that the data links you use meet their published performance figures. If they don't, then not only will the network fail to meet its performance goals, but you'll also have to retransmit data when a connected terminal or computer detects data blocks that contain errors.

To find out whether a data link meets its specifications, you can use bit-error-rate testers, which now allow you to make in-service or out-of-service error-performance checks on synchronous, asynchronous, or isochronous (recovered clock) data links operating at bit rates from less than 100 bps to 15M bps. To assist you in interpreting their results, these testers provide graphical output of recorded error-performance parameters, which lets you quickly spot trends and events that occur during test periods of hours or even days.

Capable of generating and analyzing structured data, *the Marconi 2871 can perform drop-and-insert tests on CCITT X.50 data networks.*

Unlike other error-checking procedures, bit-error analysis provides a true measure of a data link's performance. The CRC (cyclic redundancy check) error checking provided by communications software in data-terminal equipment, for example, hides many of the imperfections in communications links. If a check on the CRC code sent after each data block reveals the presence of data errors in the block, the receiving end of the link requests retransmission of the entire data block. Therefore, you can't judge the data throughput of the communications link merely by the amount of data transmitted and received by terminal and computer equipment at either end of the link, because the link may actually be carrying significant overhead in the form of retransmitted data.

As you increase the amount of data being transmitted over the link, this overhead will appear in the form of poor response times from the terminal equipment. Perhaps, though, your company's accounting department will spot the problem first in the line charges incurred during the retransmission of faulty data.

Bit-error-rate testers, however, provide a true measure of a communications link's performance, because they examine the actual data on the link. Unlike other means of assessing the link's performance (for example, examining analog impairment characteristics or bipolar violations), bit-error analysis is independent of the communications medium and of the coding method used to represent the data. It makes no difference to a bit-error tester whether the data is carried on twisted-pair wiring, coaxial cable, fiber-optic cable, or radio links, all of which may be used in various sections of a long-haul data link.

Bit-error-rate testers that are specific to a particular type of data link have been available for some time, but it's only recently that general-purpose models have become available. These general-purpose units—such as Telecommunications Techniques' Fireberd 6000 and Marconi Instruments' 2871 bit-error-rate testers, both of which were introduced within the last year, and Phoenix Microsystems' 5500, which has been available for about two years—are capable of determining error-performance parameters on a wide variety of data-communications links. They log errors in real time.

Unlike earlier bit-error-rate testers and low-cost models, these three

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CIRCLE NO 94

testers measure error-performance parameters that are in accord with internationally agreed-upon performance criteria, and they time-correlate these parameters to assist you in tracking down the sources of errors induced by the data link.

Data rates and interfaces

With the $8495 Fireberd 6000, you can test synchronous data links operating at bit rates between 50 and 15M bps, asynchronous links between 50 and 20k bps, and isochronous links between 50 to 520k bps. The unit has a built-in RS-232C interface and additional plug-ins that include V.10/V.11, V.35, TTL, WECO-303, RS-449, MIL-188, DS0, DS1, DS1C, and DS2 interfaces, as well as 64k-, 2.048M-, or 8.448M-bps G.703 interfaces.

The Phoenix 5500 operates at bit rates from 75 to 13M bps. The $5995 instrument comes with an RS-232C interface. The company offers additional plug-in interfaces to RS-449; V.35; Bell 303; TTL; DDS; T1/T1C; T2; and 64k-, 2.048M-, or 8.448M-bps G.703 data links. The interfaces range in price from $295 to $995. An optional $2495 module-switching unit houses as many as 16 of these interface modules and allows you to select an individual interface either locally, from the front panel of the module-switching unit, or remotely, from the 5500 mainframe.

The £5500 Marconi 2871 operates at bit rates between 50 and 150k bps. Although the 150k-bps upper limit won't get you directly onto 1.544M-bps T1 links or 2.048M- or 8.448M-bps G.703 links, it is sufficient to handle these links on a channel-by-channel basis if they're time-division multiplexed. The instrument targets 64k-bps applications. Its front panel incorporates codirectional, contradirectional, and binary interfaces; a plug-in RS-232C interface is also supplied with the instrument. RS-449, X.21, and V.35 interfaces are available for the 2871.

Featuring a CRT display and softkey control, *the Phoenix 5500 can measure 23 error-performance parameters, as well as clock frequency, asynchronous bit rate, event time, bias distortion, and phase jitter.*

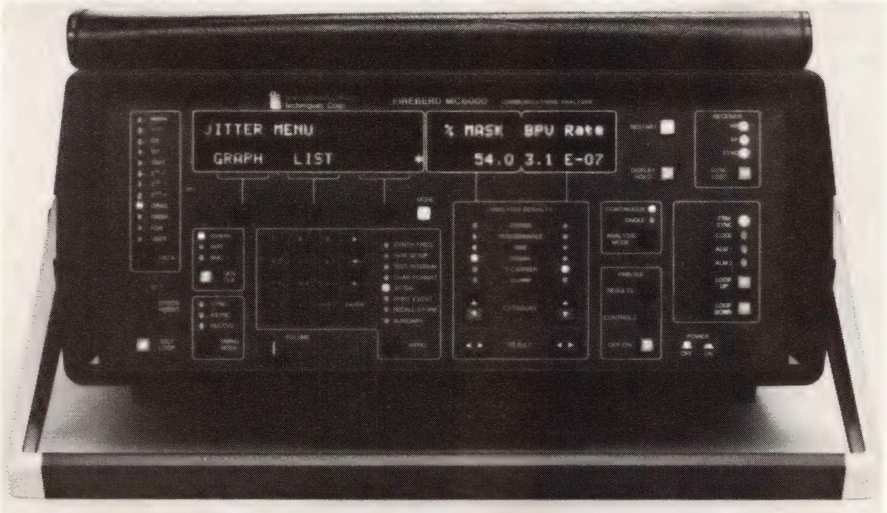
Although all these instruments take the traditional bit-error-ratio measurement (the ratio of faulty data bits to the total number of bits carried on the link), they also take several time-related measurements. These time-related measurements are necessary because the distribution of data errors in real time has an important influence on the degree to which the errors affect data transmission.

For example, consider a 64k-bps link that's transmitting data in 1024-bit blocks. If this link, measured over a period of 1 sec, has a bit-error ratio of 1×10^{-3}, then approximately 64 single-bit errors will have been recorded. If all these errors occur in a single burst, they may affect only one or two data blocks, so they'll cause minimal transmission overhead: You'll need to retransmit only one or two blocks of information. However, if the data errors are evenly distributed throughout the 1-sec period, they could easily cause one error in every data block. In this case, you'd have to retransmit all 64 data blocks. If this pattern of errors persists during the period of retransmission, no good data is transmitted over the link. Hence, different error distributions affect data links in different ways.

Because it's impossible to eliminate errors induced by data links, it's important to determine the acceptable level of error. The traditional method of measuring only the long-term bit-error ratio on the link is inadequate for this purpose, because it tells you nothing about the distribution of the errors.

To help establish a standard that would promote more accurate assessment of data-link performance, the CCITT published the G.821 recommendations. These recommendations relate to a long-haul (27,500 km), 64k-bps digital link, which is emerging as a standard building block for future communications systems, including the Integrated Services Digital Network (ISDN). Because the recommendations include a means of apportioning the performance parameters among various grades of connections, however, you can apply the general principles of the G.821 recommendations to links of other types.

Because 64k-bps links are intended to carry digitally encoded



Operating to bit rates as high as 15M bps, *the Fireberd 6000 from Telecommunications Techniques Corp performs error analysis, timing analysis, and jitter testing, and it generates structured data to test T1 networks.*

voice and data information, the performance measurements recommended by G.821 include parameters that relate the effect of the error distribution to the type of information (voice or data) on the link. Bursts of errors lasting for a short time—less than 1 sec, for example—tend to corrupt voice information, making it unintelligible, although they have a much less disastrous effect on data transmissions.

The G.821 recommendations specify that error in voice links be measured in terms of "severely errored seconds" and "degraded minutes." Severely errored seconds occur when the bit-error ratio exceeds 1×10^{-3} for a 1-sec period, usually resulting in unintelligible speech. Degraded minutes occur when the bit-error ratio, averaged over a period of one minute, exceeds 1×10^{-6}. Because the degraded-minutes parameter is intended to provide a measure of the general voice-data performance of the link, periods of severely errored seconds are excluded from the calculation of degraded minutes.

For data communications, the important measurement parameter is the "errored second," a 1-sec period during which one or more errors are detected. The errored second provides a measure of the randomly distributed data errors.

Calculation of both degraded minutes and errored seconds excludes periods for which the link is considered unavailable. The link is considered to be unavailable during a period beginning with 10 or more consecutive severely errored seconds and ending immediately before 10 consecutive seconds that are not severely errored.

The G.821 document also recommends an acceptable level of link performance in terms of the proportion of available time occupied by degraded minutes, errored seconds, and severely errored seconds. A link is acceptable if its degraded minutes constitute less than 10% of available time, its errored seconds constitute less than 8% of available time, and its severely errored seconds constitute less than 0.2% of available time. Because, in practice, the three parameters are interrelated, an acceptable link must satisfy all three percentage limits concurrently. By specifying acceptable link performance in this way, you're not constrained to any particular measurement period, although the G.821 document recommends one month as a suitable reference period for monitoring a long-haul 64k-bps link.

G.821 testing capabilities are a standard feature of the £5500 Marconi 2871. The unit has a special CRT display page that indicates all the G.821 performance parameters and gives additional information on the bit-error ratio (excluding severely errored seconds) and on the number and distribution of periods of unavailable time (breaks). In addition, the tester lets you modify the bit-error ratios and time periods used to qualify unavailable time, severely errored periods, and degraded periods. Therefore, you can modify the tests to suit data links operating at bits rates other than 64k bps. The 2871 can continuously monitor G.821 parameters for a period of approximately 180 days.

G.821 testing is also a standard feature of the $8495 Fireberd 6000 testers shipped since January 1987. Although the 6000 operates with the fixed G.821 bit-error-ratio thresholds, you can use it with any interface card and at any data rate. You can instruct the instrument to print a hard copy that includes only G.821 parameters or a printout that includes other test parameters as well. In addition, you can program the instrument to print error-performance parameters when specific events occur—for example, when the tester detects unavailable time.

For the Phoenix 5500, G.821 test capability is an option. The option changes the tester's designation to 5501 and increases the 5500's $5995 price tag by $600. The option also adds a special display page devoted to G.821 test parameters. As does the Marconi 2871, the Phoenix 5501 lets you display additional information relating to the occurrence and distribution of periods of unavailable time (breaks). (The similarity between these additional facilities on the Phoenix 5501 and the Marconi 2871 is no coincidence: In both cases the additional facilities were designed to meet the testing requirements of British Telecom.)

The 5501 also allows you to modify the error ratios used in the evaluation of severely errored seconds

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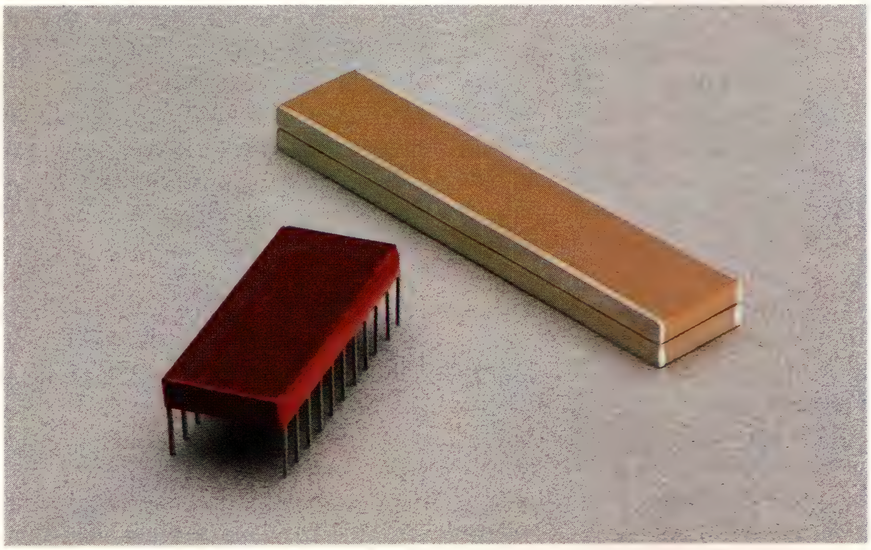

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The theoretical output filter capacitor values of SMPS's are in the range of 6-10 μF/amp at 40 KHz and drop to less than 1 μF/amp at 1 MHz. Most electrolytic applications use 10 to 100 times the theoretical value in order to obtain lower ESR from paralleling many capacitors. But the low inherent ESR of SupraCap MLC capacitors, typically less than 10 mΩ, means that users can select capacitance values close to the theoretical and enjoy low ripple voltage and less self-heating of the capacitor itself.

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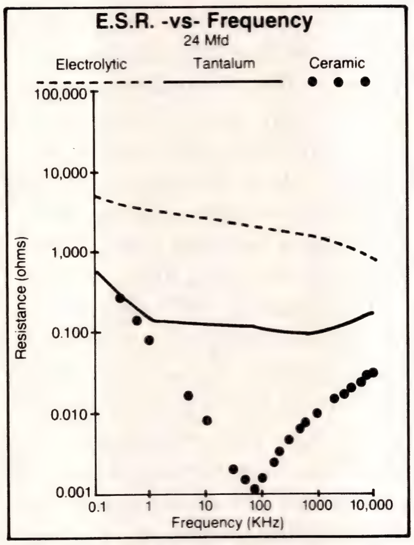

Figure 1

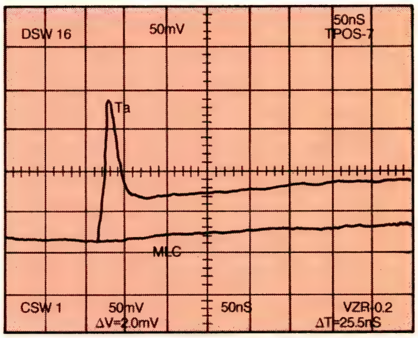

Figure 2

Discussion

By achieving low ESR and ESL at lower capacitance values, SupraCap MLCs are a desirable alternative to electrolytic and tantalum capacitors in many SMPS applications. In fact, when the theoretical requirements of the output filter are less than 50 μF, the ceramic MLC is a preferred substitute based on its performance.

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and degraded minutes so that you can apply G.821 testing techniques to other links. Unlike the Marconi 2871, which allows you to select only bit-error-ratio thresholds of 10^{-5}, 10^{-6}, or 10^{-7} for degraded minutes and 10^{-2}, 10^{-3}, 10^{-4}, or 10^{-5} for severely errored seconds, the 5501 allows you to enter the threshold value as an integer that represents the number of errors applicable over the 1-minute or 1-sec interval. Thus, the 5501 gives you greater flexibility in determining the threshold levels. However, the Phoenix 5501 doesn't allow you to extend the measurement periods to degraded 10-minute or severely errored 10-sec periods, as the Marconi 2871 does.

Clearly, to establish G.821-type performance criteria for a link, you need to monitor the link for a considerable time. Further, long-term monitoring of data links may be necessary for another reason: Most data-link problems are intermittent, occurring only at particular times of day, or when particular events occur on the network. Such long-term monitoring would be expensive if you had to pay highly trained test engineers, possibly working odd hours, to do it. However, a bit-error-rate tester that logs a data link's performance over a period of hours or days would be an attractive alternative.

The Marconi 2871, Fireberd, or Phoenix 5500/5501 testers can monitor data links continuously for a number of hours, but this number depends on the bit rate of the transmission and the number of parameters you're trying to measure. If you regularly dump the information to a printer, you can continue monitoring data links indefinitely.

Histograms ease analysis

When a problem occurs, you can examine the tester's measurement parameters minute by minute to investigate what happened. By knowing exactly when bit errors, synch losses, or local power failures occurred, you can greatly reduce the detective work you must do to discover the cause of the errors. But sifting through 30 or 60 hours' worth of error-analysis printouts can still be a time-consuming task, and it's often difficult to spot trends in a long list of results. To ease your task of analyzing the link's error performance, all of these instruments are capable of displaying or printing out their results in the form of histograms, which make it easier for you to spot trends or unique events.

The Phoenix 5500/5501 allows you to time-correlate four of nine error parameters for subsequent display as histograms. If you select only one of these parameters, the instrument can record as many as 60 hours of data. You can select the histogram resolution to be either one hour or one minute. The histogram display features two movable cursors that allow you to scroll forwards or backwards through the recorded data and to define the displayed time window. The 5500/5501 also keeps track of any synch losses and local power failures that occur during testing. It's important to know when power failures occur, because they are a common cause of error bursts on the data link.

The Marconi 2871 allows you to display a histogram of errors recorded while you're running test-pattern or framing-bit error measurements. The histogram, which has 1-hour resolution, displays the number of errors detected over a selected 30-hour period. You can expand the histogram to show the errors that occurred during any 1-hour period; this histogram has a measurement resolution of as little as 1 minute.

In addition, the 2871 indicates, below its horizontal time axis, periods when loss of synch occurred, periods when the test was temporarily suspended by operator intervention, and periods when local power failures were detected. A movable histogram cursor and a text area on the screen provide you with detailed information on various error parameters.

Although Telecommunications Techniques' Fireberd 6000 doesn't have a CRT display, it lets you print (on an Epson-compatible dot-addressable printer) histograms of error-performance data accumulated over test periods as long as 60 hours. When synch losses occur, you can program the instrument to respond by clearing accumulated data, halting, or continuing with data accumulation. In addition, you can select the synch-loss threshold to be one of three bit-error ratios. The Fireberd 6000 also logs local power failures.

Out-of-service testing

If you operate your own communications network or leased phone lines, you can take these lines out of service to test them. To perform out-of-service testing, you usually loop back the data link at its distant end and use a bit-error-rate tester to compare the transmitted and received data patterns on the other end of the link.

Alternatively, you can deploy separate bit-error-rate testers, one at each end of the data link. This technique also allows you to carry out half-duplex, end-to-end testing. The transmitted data pattern generated by the bit-error-rate testers is normally a pseudorandom binary sequence (PRBS) that typically ranges in length from a few tens or hundreds of bits to $2^{23}-1$ bits. In general, the higher the data rate of the link, the longer the PRBS pattern required to test it. You can also normally select an all-ones, all-zeros, or alternating one/zero test pattern, or a user-programmable test pattern.

In-service monitoring

If you control the entire network, you might also have the opportunity to loop back at several points along the communications link, or to reposition transmitting and receiving bit-error-rate testers, thus making

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MSA-0204	4.0	11.0	6.5	4.0	B	1.90
MSA-0370	4.5	12.5	5.5	10.0	A	16.10
MSA-0420	3.5	8.5	7.0	15.0	C	18.45
MSA-0685	4.0	16.5	3.0	1.5	D	1.30
MSA-0835	6.0	23.5	3.0	12.5	E	7.80
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it easier to isolate the section of the data link on which the data errors are occurring. However, even if you are able to perform out-of-service testing, you might want to avoid doing so because it would inevitably interrupt the link's availability to your computer users.

You'll also want to consider the fact that network data is often structured, which means that it contains fixed patterns of framing bits inserted at regular bit intervals in the data, so that data-terminal equipment can synchronize to the transmitted data stream. To perform loop-back testing on structured data links, your bit-error-rate tester must be capable of transmitting framed data so that your test patterns appear to the network as live traffic.

The very presence of a fixed pattern of framing bits that is already embedded in the network's data, however, gives you the alternative of performing in-service bit-error-rate testing without having to loop back the link. Your bit-error-rate tester can synchronize itself to the data stream in the same way that any other data-terminal equipment does, and it can check to see if any of the received fixed-pattern framing bits are in error. Because, statistically, random errors induced by the link affect framing bits in exactly the same way that they affect data bits, you can extrapolate the bit-error-ratio parameters for framing bits to all data on the link.

The Marconi 2871 can both transmit and receive structured data with 6+2 (one framing bit, six data bits, and one status bit) or 8+2 (one framing bit, eight data bits, and one status bit) framing. The transmitted data bits can be any of the instrument's test patterns. When you're driving a 64k-bps link with 6+2 structured data, the 2871 automatically reiterates the data an appropriate number of times to produce a transmitted data rate of 64k bps.

Tester checks X.50 channels

The 2871 also simulates structured data for use on CCITT X.50 multiplexed channel systems. The X.50 recommendations cover the multiplexing of several synchronous data channels, operating at bit rates of between 0.6 and 9.6k bps, onto a single 64k-bps channel. Using any of these bit rates, the 2871 generates X.50 structured data that has the test pattern in any selected channel. You can set the remaining channels to all ones, all zeros, or a 2^7-1 PRBS.

You can also perform drop-and-insert testing on X.50 systems by inserting test-pattern data in a single channel of an externally generated X.50 signal, such as X.50 live traffic. This drop-and-insert facility allows you to test one channel of an X.50 system without intruding on the rest of the system traffic. For all structured traffic, you can program the 2871 to check the data and framing bits, or only the framing bits, for error.

The Phoenix 5500 and 5501 require a suitable interface before they can generate structured data. The manufacturer offers an optional interface that can generate test patterns for use on D4-framed T1 networks, and it plans to introduce a T1 interface with extended-superframe-format framing (F_e framing) capability this quarter. Also slated for introduction this quarter is an interface module that generates framed data for use on European 2.048M-bps links. In addition to generating framed data, these interfaces examine the received framing information to determine the occurrence of synch losses and alarm conditions that are encoded in the framing information.

Telecommunications Techniques' Fireberd 6000 produces D4-framed and extended-superframe-format data for transmission on T1 networks. It can also provide in-service monitoring facilities by performing framing and CRC-error analysis on live traffic.

Besides measuring parameters derived from the bit-error ratio, you may also need to test your data links for phase jitter. Phase jitter is the short-term displacement of data pulses from their ideal timing in relation to the local receive clock oscillator. Phase jitter is particularly relevant to links having high data rates, such as 1.544M-bps T1 links. If phase jitter is present in large-enough amounts, it can cause error bursts and timing slips. Typical sources of phase jitter are T1 repeaters, multiplexers, and demultiplexers. Phase jitter is measured by the peak-to-peak value of the phase error and by its frequency spectrum (over a 10-Hz to 40-kHz bandwidth for a 1.544M-bps link).

Both the Phoenix 5500/5501 and

For more information . . .

For more information on the bit-error-rate testers described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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the TTC Fireberd 6000 have options that allow you to measure the amount of phase jitter in a received T1 data signal. Both instruments can provide their test data graphically in the form of a spectrum analysis over the 10-Hz to 40-kHz bandwidth, together with a jitter mask (or limit curve) to tell you whether or not the link is within specified limits. The Fireberd 6000 allows you to select PUB-62411-1983 or -1985, PUB-41451 and -43801, or CCITT-0.171 jitter masks. The Phoenix 5500/5501 has a PUB-62411-1983 mask and a mask suitable for CCITT-G.703 2.048M-bps links; the manufacturer plans to add a software update to the 5500/5501 that will allow you to define your own jitter masks.

Both units allow you to inject a programmed amount of jitter into the transmitted data signal, an operation that's useful when you want to test how much phase jitter your data link can tolerate. This year, the manufacturer plans to introduce enhancements to the Fireberd 6000's jitter-analysis capabilities that will extend its use to data links operating at other bit rates.

Remote monitoring

All three of these bit-error-rate testers feature RS-232C and IEEE-488 instrument-control interfaces, which let you remotely control their test functions and interrogate their test results.

The presence of an RS-232C control interface is of special significance in bit-error-rate testers because it opens the possibility of remote, unattended network monitoring. You can position the bit-error-rate tester at any suitable point in the network and control its operation via dial-up access to a modem connected to its RS-232C control interface.

Once the tests are complete, you can download the results via the same route. For example, if you link a tester into each of the network's cross-connect switch bays, you can sequentially monitor each network data link by performing in-service checks. When you find a link that appears to have problems, you can reroute network traffic and take that link out of service for comprehensive testing. By remotely accessing the testers via dial-up lines, you can control the entire network-monitoring system from a central computer.

You might be tempted to think that $5000 to $8000 is too much to spend on a piece of test equipment that will tell you most of the time that everything is okay, but such is not the case. If your high-performance bit-error-rate tester detects even one or two high-capacity links that are performing below specification, it could quickly save you a lot of data-transmission overhead.

What's more, bit-error-rate testers are useful for more than just testing data links. You can also use them to test data-circuit-terminating equipment at either end of a communications link. If you manufacture modems, for example, you can test them on the production line by looping back the phone-line side of each modem and connecting a bit-error-rate tester to the modem's digital side to check the transmitted and received data. In such an application, the testers' IEEE-488 interfaces would allow you to automate the entire test operation. **EDN**

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1. CCITT Recommendation G.821, *Error Performance of an International Digital Connection Forming Part of an Integrated Services Digital Network*, Fascicle III.3, Geneva, Switzerland, 1980.

2. Sciulli, Joseph and John Peeler, "Error Analysis on Digital Communications Links," *Telecommunications Magazine*, Volume 19, Number 3, 1985.

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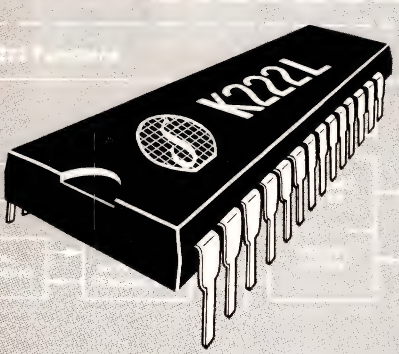

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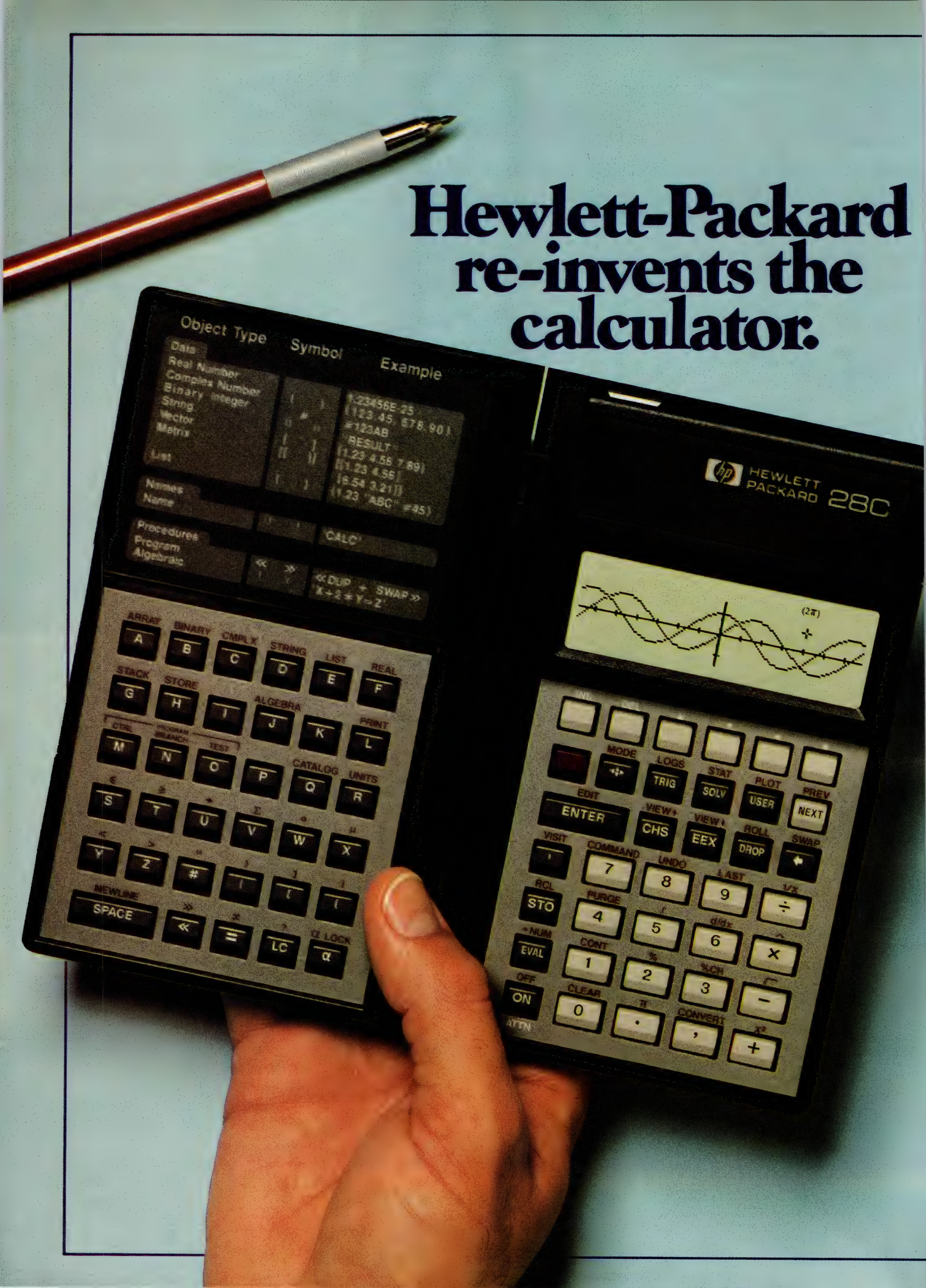
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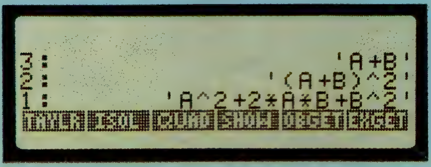
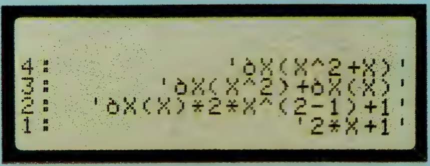


```
3:                    'A+B'
2:                '(A+B)^2'
1:      'A^2+2*A*B+B^2'
TAYLR ISOL QUAD SHOW OBGET EXGET
```

THE FIRST CALCULATOR THAT DOES SYMBOLIC CALCULUS



```
4:              'ðX(X^2+X)'
3:        'ðX(X^2)+ðX(X)'
2:  'ðX(X)*2*X^(2-1)+1'
1:                '2*X+1'
```

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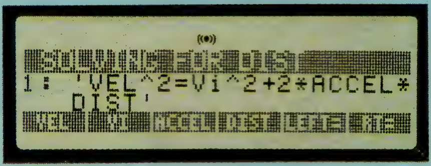

```
SOLVING FOR DIST
1: 'VEL^2=Vi^2+2*ACCEL*
    DIST'
VEL  VI  ACCEL DIST LEFT= RT=
```

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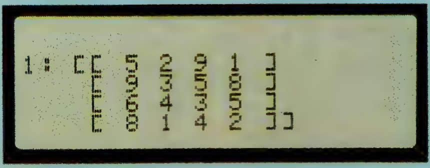
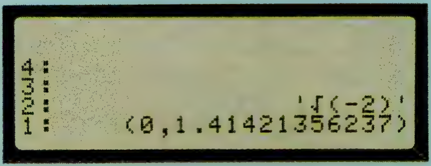


```
1: [[ 5  2  9  1 ]
    [ 9  3  5  8 ]
    [ 6  4  3  5 ]
    [ 8  1  4  2 ]]
```

THE FIRST CALCULATOR THAT DOES COMPLEX NUMBER ARITHMETIC AS EASILY AS FOUR-FUNCTION MATH



```
4:
3:
2:                 '√(-2)'
1:     (0,1.41421356237)
```

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CIRCLE NO 99

ISSCC '87 will explore IC design in a restructured semiconductor industry

David Shear, *Regional Editor*

The shift in the semiconductor industry will bring about a shift in the traditional role of the IC designer, maintains Robert Brodersen, the keynote speaker at this year's International Solid State Circuits Conference (ISSCC), which will take place February 25 through 27 in New York, NY. According to Brodersen (of the University of California at Berkeley), today's semiconductor industry has changed: Companies are focusing on narrower market segments, which allow them significant profit margins without requiring them to cut manufacturing costs too drastically. The IC designer's task will change in accordance with the changing value of the integrated circuit in today's semiconductor industry.

The value of the chip now, Brodersen believes, lies in its implemented algorithms and architectures and in the time to market. The IC designer's task in this restructured industry will no longer be to create new compact memory-storage cells and dense layouts, Brodersen maintains, but to identify new applications for ICs and new architectures that will make these applications possible.

In his talk, Brodersen will also examine the problem of the enormous complexity of designs. Engineers have frequently tried to attack this problem by the inefficient method of applying more manpower, instead of using efficient software tools, he believes. To solve the problem, Brodersen will propose a new design methodology that would merge traditional designers and designers using CAD into a more homogeneous group of designers and tool developers.

Besides changes in the traditional categories of engineering designers, Brodersen foresees a major upheaval in the design style currently in use in the analog sector. The integration of analog circuit functions, for instance, is becoming increasingly critical for applications such as telecommunications. He believes that the traditional analog-design techniques based on precision components will be replaced by techniques that are more compatible with the integration of systems on a chip.

Technical sessions

Among the more than 100 papers to be presented at ISSCC '87 will be reports on as-yet-unreleased technological advancements in memory ICs, microprocessors, converters, and many other areas. The technological advancements in these areas come mainly in the form of higher speeds, greater densities, and lower power.

Papers in **session 1**, for instance, will describe 4M-bit dynamic RAMs with sub-100-nsec access times. Participants in **session 2** will discuss five different 32-bit microprocessor designs with various combinations of on-chip memory for instruction/data-cache and translation-look-ahead buffers. Four of these designs are RISC (reduced-instruction-set computer) implementations; one is compatible with a minicomputer instruction set.

Session 16 will describe a chip set for a massively parallel architecture. One of the chips contains 32 processors and performs 320 million 4-bit operations per second. **Session 4** will present a 7.4-nsec CMOS 16×16-bit multiplier, a bipolar/CMOS 300-MHz video shift register, and a 1-nsec Josephson ALU with an average gate delay of about 11.5 psec.

Continuing the discussion of speed enhancements will be **session 11,** in which speakers will describe fast static RAMs. Two of the parts they will discuss are a 5-nsec, 64k-bit ECL static RAM and a 1-nsec, 4k-bit GaAs static RAM. Participants in **session 7** will report on 1M-bit (64k×16 bits) and 4M-bit (512k×8 bits) CMOS EPROMs and will give information on a 256k-bit CMOS EEPROM with a million-cycle endurance. **Session 9** will present an 8-bit, 350-MHz flash A/D converter and a 1-GHz, 6-bit A/D-converter system. **Session 20** will highlight a 3-μm CMOS chip that's capable of generating 2 million chess moves per second.

New developments in the analog world will also be explored at ISSCC '87. For example, papers in **session 3** will describe a sampled-data analog circuit. Reports in the session will examine GaAs switched-capacitor filters having sampling rates as high as 300 MHz and signal frequencies as high as 20 MHz; a GaAs, 8-nsec monolithic S/H amplifier with a 170-MHz bandwidth; a single-chip analog-interface processor containing an 8-channel multiplexer, a programmable instrumentation amplifier, a bandgap reference, and interface circuitry; and two oversampling A/D converters, one with an internal digital filter and one with rail-to-rail input capability.

Papers in **session 14** will cover advancements in wideband amplifiers. For example, one report will examine a matched-impedance NMOS amplifier with a bandwidth of 758 MHz. Two others will focus on a multistage NMOS AGC amplifier and a 4G-bit/sec amplifier, both

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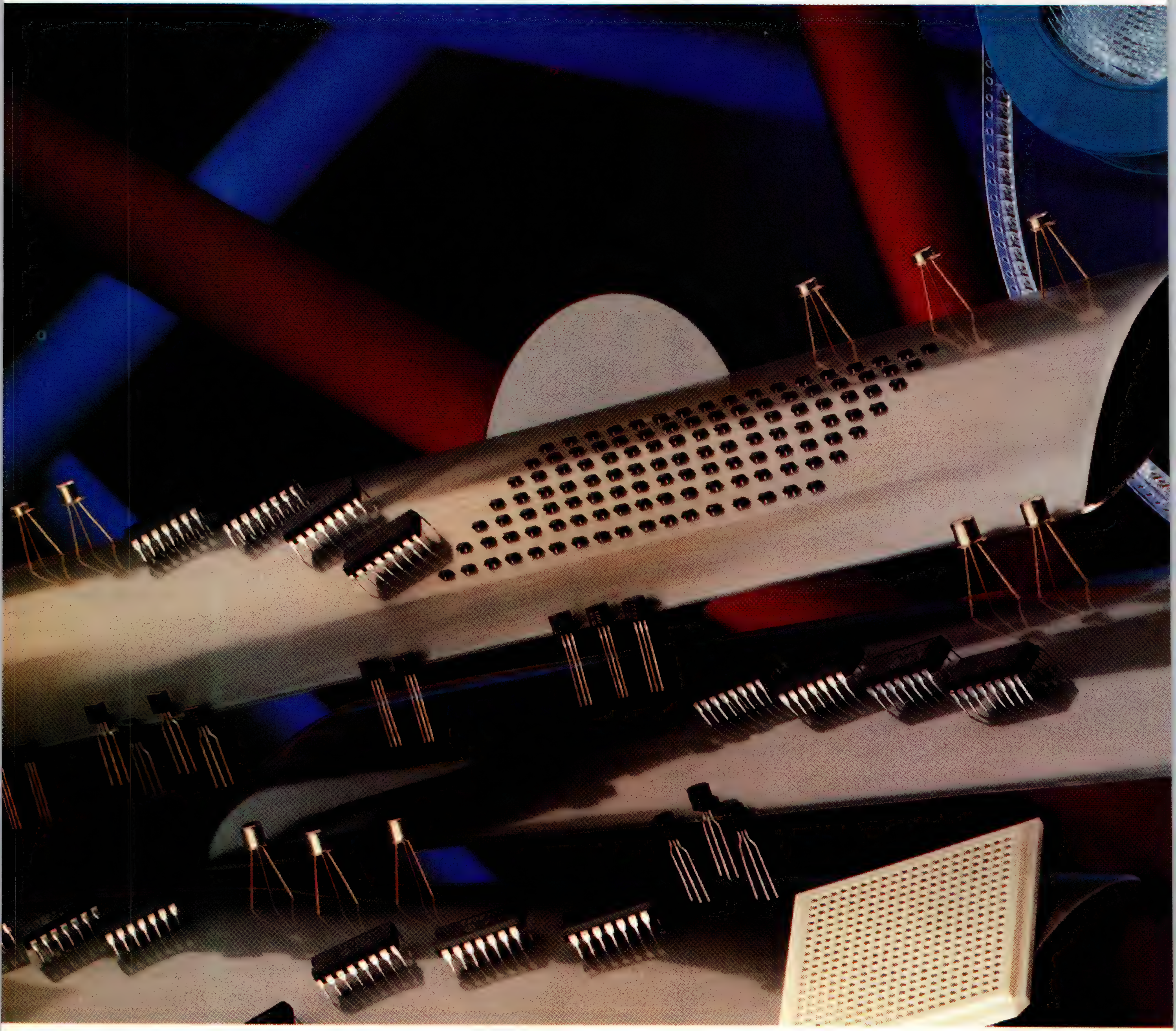

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CIRCLE NO 109

ISSCC '87 registration details

The International Solid State Circuits Conference will take place February 25 through 27 at the New York Hilton Hotel, New York, NY. Consult the **schedule** for the times and locations of the technical sessions and informal discussions.

You can register for the conference on the Promenade (second floor) between 4:00 and 8:00 PM Tuesday, between 8:00 AM and 4:00 PM Wednesday and Thursday, and between 8:00 and 11:00 AM Friday.

Advance registration fees (before February 16, 1987) are $110 for IEEE members and $130 for nonmembers. After February 16, those registration costs will be $120 and $140, respectively. Each registrant will receive a copy of the *Digest of Technical Papers;* additional copies cost $70 for IEEE members, $80 for nonmembers, and $20 for students who attend the conference.

For additional information, contact Lewis Winner at 301 Almeria Ave, Coral Gables, FL 33134. Phone (305) 446-8193.

ISSCC '87 AT NEW YORK HILTON HOTEL/NEW YORK, NY

	TIME	GRAND BALLROOM WEST	GRAND BALLROOM EAST	TRIANON BALLROOM	RHINELANDER SOUTH	PETIT TRIANON
WEDNESDAY FEBRUARY 25	9:00 AM 11:45 AM	SESSION I MEGABIT DRAMs	SESSION II 32-BIT MICROPROCESSORS	SESSION III SAMPLED-DATA ANALOG CIRCUITS	SESSION IV HIGH-SPEED-CIRCUIT TECHNOLOGY	—
	1:30 PM 2:05 PM	SESSION V FORMAL OPENING		—	—	—
	2:10 PM 2:50 PM	SESSION VI KEYNOTE ADDRESS		—	—	—
	3:20 PM 6:00 PM	SESSION VII NONVOLATILE MEMORY	SESSION VIII MICROPROCESSOR-DESIGN METHODOLOGY	SESSION IX HIGH-SPEED ADCs	SESSION X IMAGE SENSORS AND PROCESSING CIRCUITS	—
		INFORMAL DISCUSSION SESSIONS				
	8:00 PM	WE 1 DRAM CELL STRUCTURES AND TECHNOLOGIES	WE 2 ASIC ARCHITECTURES FOR THE '90s	WE 3 NEXT-GENERATION IC TECHNOLOGY FOR ANALOG/DIGITAL VLSI	WE 4 FUTURE TRENDS IN NONVOLATILE MEMORIES	WE 5 DIRECTIONS IN SMART POWER ICs
THURSDAY FEBRUARY 26	9:00 AM 12:15 PM	SESSION XI FAST SRAMs	SESSION XII SEMICUSTOM-ARRAY DESIGN	SESSION XIII DIGITAL SIGNAL PROCESSORS	SESSION XIV WIDEBAND AMPLIFIERS	—
	1:30 PM 5:00 PM	SESSION XV HIGH-SPEED SIGNAL PROCESSORS	SESSION XVI MICROPROCESSORS: SPECIAL PURPOSE	SESSION XVII ANALOG TECHNIQUES	SESSION XVIII TEST AND PACKAGING	—
		INFORMAL DISCUSSION SESSIONS				
	8:00 PM	THE 6 DIGITAL ICs WITH EMBEDDED MEMORY	THE 7 COMPETING TECHNOLOGIES FOR HIGH-SPEED DIGITAL SYSTEMS	THE 8 TRENDS IN DESIGN AUTOMATION FOR MIXED ANALOG/ DIGITAL ASICs	THE 9 EDUCATING FUTURE CHIP DESIGNERS	THE 10 TECHNOLOGIES FOR BROADBAND NETWORKS
FRIDAY FEB 27	9:00 AM 12:15 PM	SESSION XIX HIGH-DENSITY SRAMs	SESSION XX SPECIAL-PURPOSE ACCELERATORS	SESSION XXI TELECOMMUNICATION ICs	SESSION XXII VLSI SYSTEMS AND ARCHITECTURES	—

for use in optical systems.

Analog techniques will be the subject of **session 17.** The presentations will include reports on an analog filter with full digital programmability; a pipelined, 5-MHz, 9-bit A/D converter; an analog expert-design system; a 4-quadrant NMOS analog multiplier; a pair of GaAs ICs that form a complete front end for a VHF-UHF receiver; and a switched-capacitor voltage converter that's capable of supplying a 100-mA output current.

Advancements other than increases in speed and reduction in size, power requirements, and cost will also be explored at ISSCC '87. For example, **session 20** will present a CMOS pipeline-sorter chip that uses hierarchical redundancy and laser repair to increase IC yield by a factor of 10 while increasing the chip area by only 1.9 times.

A report in **session 12** will focus on a 6000-gate CMOS gate array with self-test and maintenance circuitry that occupies only 8% of the die. **Session 12** will also include a discussion of a silicon compiler that includes a general-purpose DSP cell.

Besides the technical sessions, ISSCC will include informal discussion sessions on Wednesday and Thursday evenings. Participants in one of the discussions, "ASIC Architectures for the '90s," will speculate on alternatives to ASICs. They will

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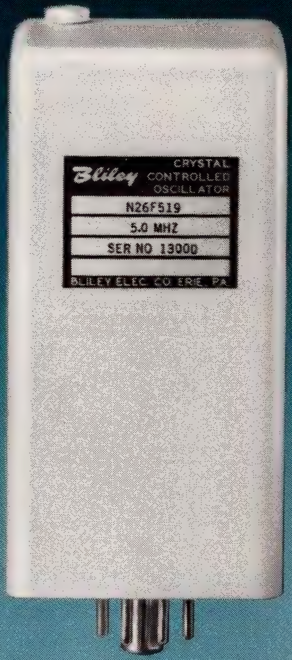

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compare MOS and bipolar arrays, standard cells, macroblocks, application-specific compilers, and other devices from the perspectives of the user, the vendor, and the CAD-tool designer. Another evening session will focus on the training that future chip designers will need.

Other informal discussions will consider the next generation of IC technology for analog/digital VLSI design, new VLSI ICs that contain large power devices, the difficulty designers have in designing and testing logic circuits with large amounts of embedded memory, and the trends in design automation for analog and mixed analog/digital ASICs. **EDN**

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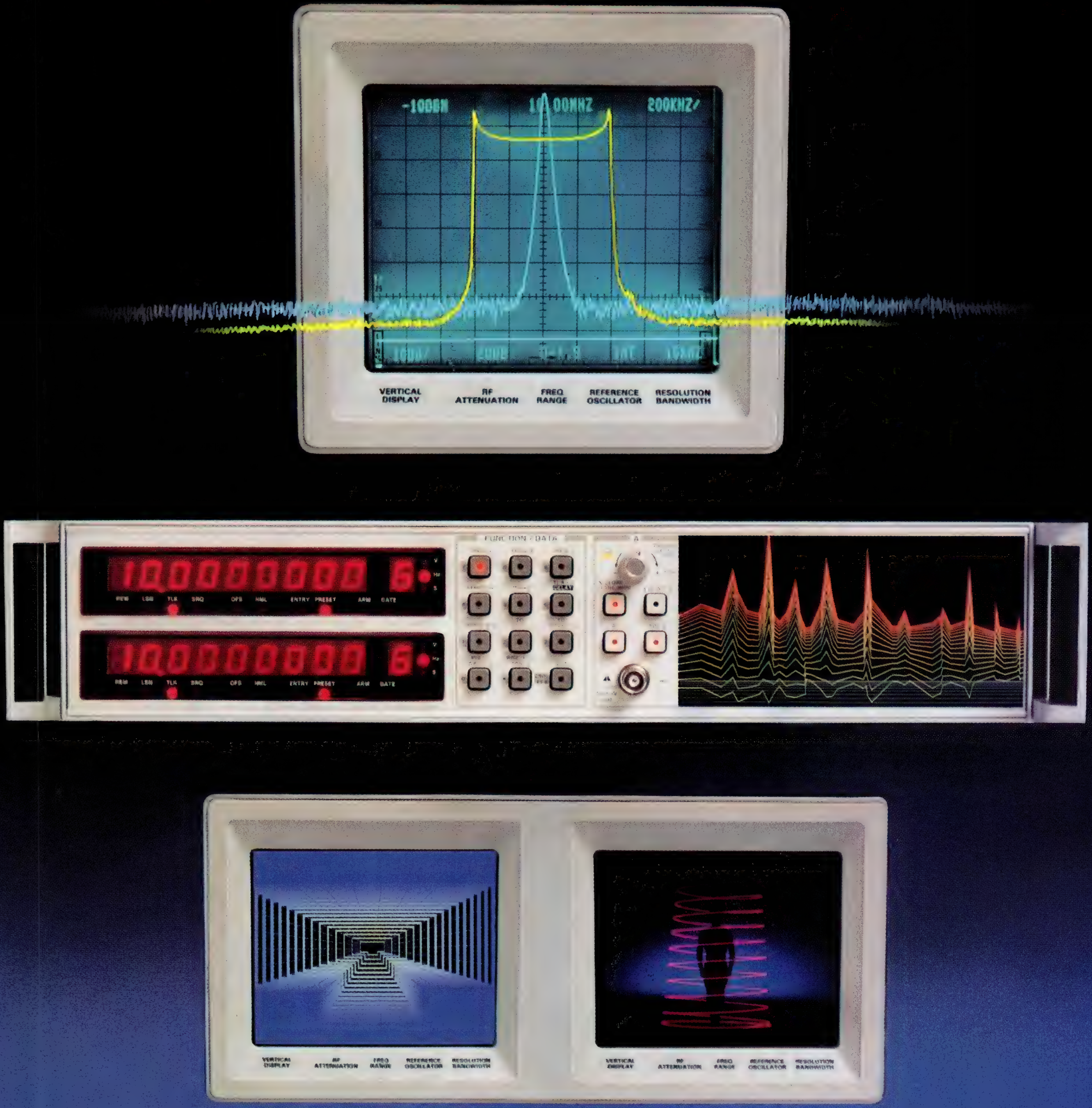

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ICL7182. Available in either a 40-pin DIP or 44-pin Small Outline package, the ICL7182 is a 101 segment LCD bargraph A/D converter. The ICL7182 offers an average power consumption of 1.8 mW, and operates over an extended temperature range.

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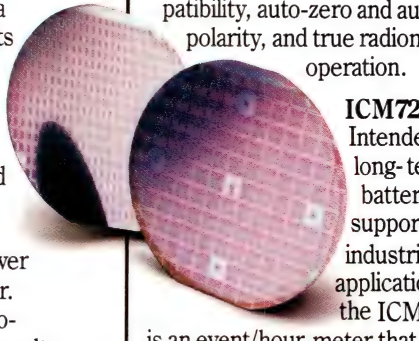
ICL7136. Designed to interface with a liquid crystal display, the ICL7136 is a high performance, very low power 3½-digit A/D converter. Its features include auto-zero to less than 1 microvolt per degree C, maximum input bias current of 10 pA, and rollover error of less than one count.

ICL7116/7117. The ICL7116 and ICL7117 are high performance, low power 3½-digit A/D converters. Both devices feature a unique "hold" reading input which allows an instrument to take a measurement, then retain the value on the display indefinitely.

ICL7135. The ICL7135 is a 4½-digit BCD output A/D converter that combines dual slope conversion reliability with ±1 in 20,000 count accuracy. Ideally suited for the visual display DVM/DPM market, the ICL7135 offers 2.0000 V fullscale compatibility, auto-zero and auto polarity, and true radiometric operation.



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ICM7216. Used to measure propogation delays, frequency, events, etc., the ICM7216 is a universal 8-digit counter/timer with direct, on-board LED display drive. Its features include 4 internal gate times, auto decimal point, and overflow indication.

ICM7226. Equal in performance to the ICM7216, the ICM7226 is a fully integrated 8-digit universal counter/timer and LED display driver. Its features include period and time interval averaging, BCD outputs and microprocessor PIA capability.

ICM7217. The ICM7217 is a 4-digit, presettable up/down counter with display driver. Designed for a variety of applications, the ICM7217 can replace up to 10 IC counters, comparators and decoder/drivers.

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Members of this series of PC/AT-compatible analog-I/O boards, which operate at various resolutions and speeds, attain throughput speeds that surpass those of any other available I/O unit. Model DT2821-G, for example, offers 16 single-ended or eight differential channels (the SE or DI mode is factory wired) of 12-bit A/D conversion at throughput rates as high as 250 kHz. The board roughly doubles the speed of its older sibling, the DT2821-F.

Although the DT2821-G is capable of a 250-kHz data-conversion rate, its speed in a computer is limited by the PC's system bandwidth. In IBM PC/ATs operating at 6- and 8-MHz clock rates, for example, the conversion rates become 180 and 220 kHz, respectively. Mounted in a Compaq 286 or Hewlett-Packard Vectra, the throughput is 235 kHz. The board can deliver its full 250-kHz throughput when you plug it into a Compaq 386 machine.

Input ranges for the DT2821-G are 0 to 10V in unipolar mode, ±5 and ±10V in bipolar operation. In addition, you can increase the sensitivity of any of these ranges by using the unit's built-in, software-controlled programmable-gain amplifier. The PGA specs gains of 1, 2, 4, and 8.

Another speed leader, the 16-bit DT2823, specs 100-kHz throughput in any PC/AT computer or compatible. The board offers four differential-input channels. Its input range is ±10V. Like all the manufacturer's boards, the DT2823 includes sample/hold circuitry.

For applications requiring selectable sensitivity, Model DT2825 provides 16 single-ended or eight differential channels (the SE or DI mode is jumper selectable) of A/D conversion, as well as a software-controlled PGA that provides gains of 1, 10, 100, and 500. Its throughput rates are 45 kHz for gains of 1 and 10 and 2.5 kHz for gains of 100 and 500.

The three boards have several common attributes. All incorporate two D/A converters that provide analog outputs; the DACs' resolution is the same as that of the units' A/D converters. The boards all provide a RAM-based channel list (and gain list in the case of the PGA units). For the A/D and D/A converters, all three boards guarantee no missing codes and monotonicity, respectively.

Additional common features include support for 5-level bus interrupt, dual-DMA-channel architecture, and a programmable pacer clock that initiates A/D or D/A conversions. Software support for the analog-I/O cards includes the company's Atlab optional subroutine package, as well as several application-specific packages. Unit prices for the DT2821-G, DT2823, and DT2825 are $2995, $2795, and $1445, respectively; $449 for Atlab.—***Bill Travis***

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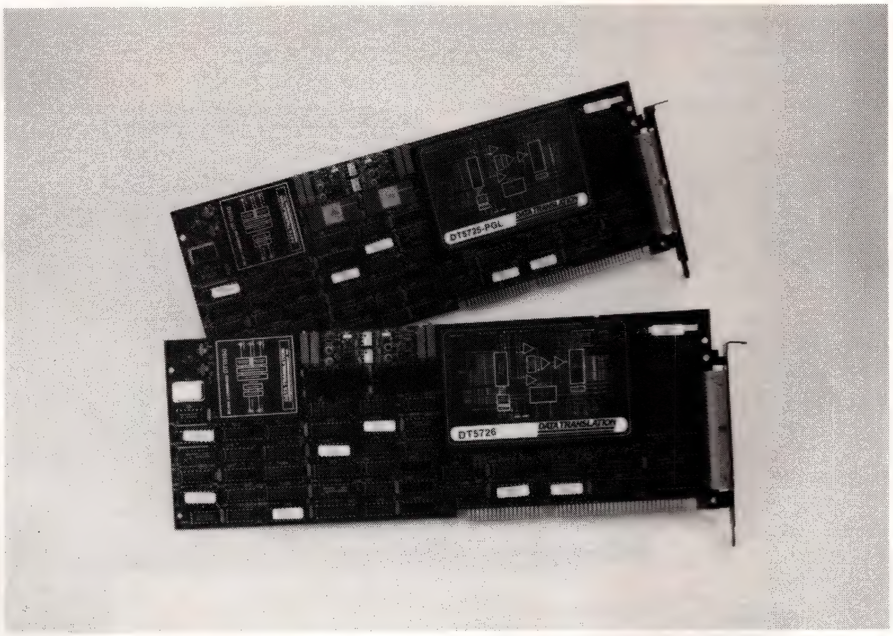

This family of analog-I/O boards, designed for the IBM PC/AT and compatibles, *pushes the computers to their limits. The 12- and 16-bit boards offer the industry's highest throughput rates. Furthermore, the devices' unequivocal no-missing-codes and monotonicity guarantees ensure that the boards provide true 12- and 16-bit resolution and linearity.*

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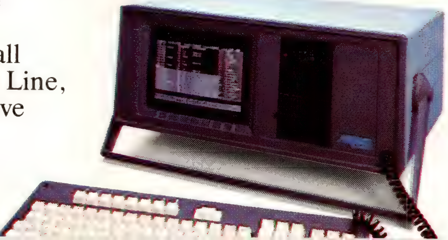
Echo is a multi-user system; but so affordable, every engineer could have his own. No sharing, no waiting, no lost man-hours. Just all the resources you need at your fingertips. One call now to the Arium Hot Line, **(800) 862-7486,** will give you all the reasons why when it comes to performance and price, nobody echoes Echo. Not from the beginning. Not now. Not ever.



ARIUM
CORPORATION

1931 Wright Circle
Anaheim, CA 92806
(714) 978-9531

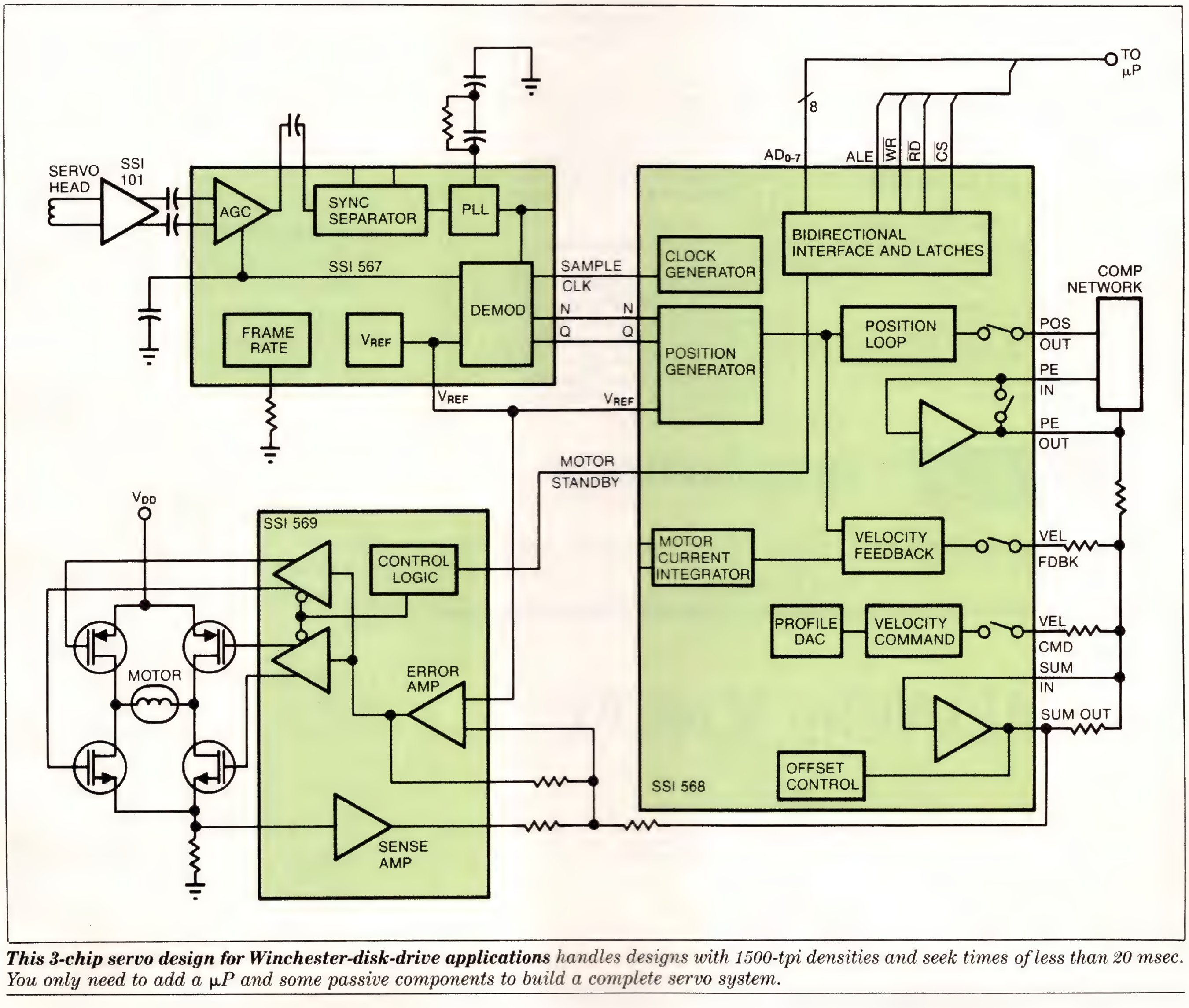
CIRCLE NO 100

Analog and digital chip set reduces discrete part count in servo systems

Servo systems like those used to control disk-drive head movement have typically required a pc board full of discrete components. The 5XX chip set, however, reduces the number of discrete components required to build such servo systems. Using the SSI 567 servo demodulator, the SSI 568 servo controller, and the SSI 569 servo motor driver, you add only a controlling μP and a handful of passive components to form a complete servo system. The chip set specifically targets Winchester-disk servo applications, but the controller and motor-driver chips will operate in general-purpose servo systems as well.

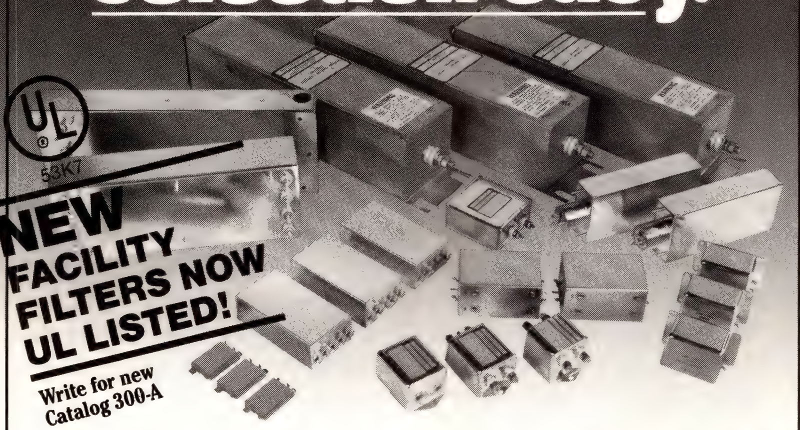
The chip set handles Winchester-disk designs that pack a maximum of 1500 tpi and operate with less than a 20-msec average seek time. Current Winchester systems spec 1200-tpi densities, and many drives only offer densities in the 500- to 800-tpi range. During the past year, drives with seek times of less than 20 msec have emerged. Though the 567/568/569 chip set is intended for such applications, it also economically serves in drives having 20- to 50-msec seek times. The system accuracy is ±2.5%.

The bipolar servo demodulator chip accepts an industry-standard dibit quadrature pattern from a disk



This 3-chip servo design for Winchester-disk-drive applications *handles designs with 1500-tpi densities and seek times of less than 20 msec. You only need to add a μP and some passive components to build a complete servo system.*

LMI makes RFI/EMI filter selection easy.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For most RFI/EMI suppression applications.
LMI filters and filter panels are now widely used in shielded rooms and cabinets, ground support equipment, computer rooms, hospital diagnostic facilities, electrical and electronic equipment, and communication centers. Write or call the LMI Application Engineering Department for additional information.

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CIRCLE NO 20

DID YOU KNOW?

Half of all EDN's
articles are staff-written.

EDN

read/write head. The chip only works in a Winchester disk drive with a dedicated servo surface. Circuitry on the chip supports automatic gain control (AGC), area detection to ensure noise immunity, and automatic zero offset. The demodulator delivers N and Q (normal and quadrature) servo signals.

The SSI 568 CMOS servo controller, which accepts the N and Q servo signals, includes a digital interface to a μP. The digital section of the chip interfaces to the analog control section via on-chip D/A converters. The IC supports both track-follow and seek modes, and it handles a speed of 500k servo frames/sec. The controller will accept standard N and Q signals from any demodulator. In fact, the company plans to offer other demodulators, including one for tribit quadrature, and you can specify or design your own demodulators for applications such as robotics.

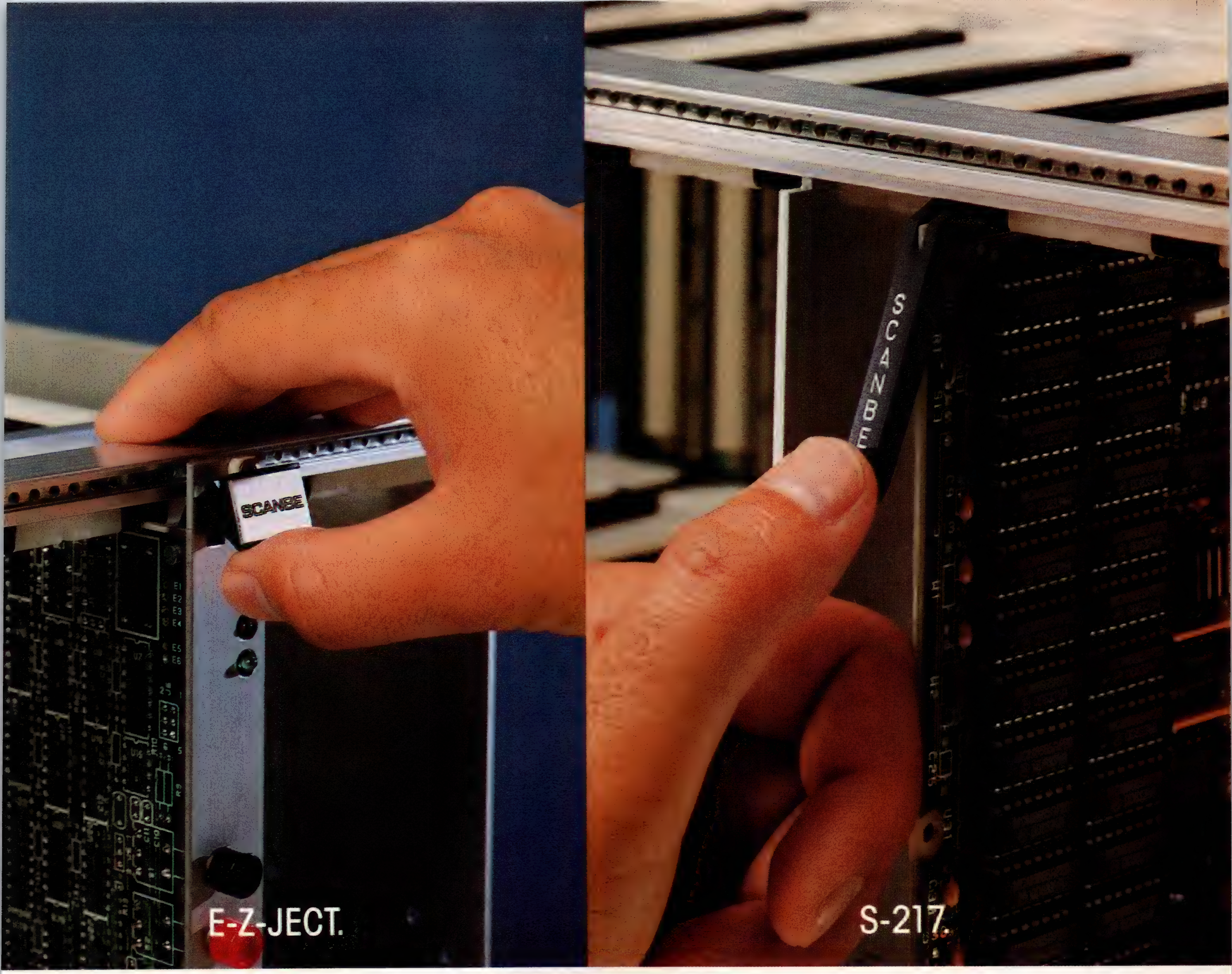
The 568 controller IC delivers an error voltage to the SSI 569 bipolar servo-motor controller chip. SSI 569 features include a linear Class B track mode, overcurrent and overvelocity protection, and enable/disable control. The IC will drive a power-MOSFET H-bridge circuit for controlling the current through a linear or rotary voice-coil motor. Low-voltage detection circuitry automatically activates motor-braking and head-retraction circuitry. In addition to using it in servo systems, you may find the chip useful in such applications as robotics and printers.

The company plans to ship samples of the chip set in the first quarter, production quantities in the second quarter. The 3-chip set will cost less than $35 (10,000). The SSI 567, 568, and 569 come in 28-, 44-, and 20-pin packages, respectively.

—Maury Wright

Silicon Systems Inc, 14351 Myford Rd, Tustin, CA, 92680. Phone (714) 731-7110.

Circle No 727



AN OPEN AND SHUT CASE FOR VME.

DIN connectors are terrific for long life and resistance to corrosion, but they also resist being plugged in and out.

Your average VME card with 192 pins, for example, may take about 24 pounds to get out of your card cage. That's a lot of force to apply with a couple of fingers.

Scanbe has two fixes for the problem. Pick one or the other, or both, depending upon your packaging situation:

E-Z-JECT is a replacement for a standard VME front panel. It has a hinged handle that lets you pop out a VME card from its backplane without the yanking and struggling you're used to. It works in any standard VME card rack. It's the way the VME front panel should have been designed in the first place.

S-217 is an injector/ejector system that gives you a lot of leverage—about 3.5 to 1—for the easiest insertion and ejection of cards without front panels. It's a great help for 6U cards and it's the ultimate answer if you're using 9U cards. (If you're using Eurocards, you should be talking to us about our versatile standard and mixed-height Eurocard cages.)

Or you can use both. Our newest VME card cages let you intermix S-217 and E-Z-JECT.

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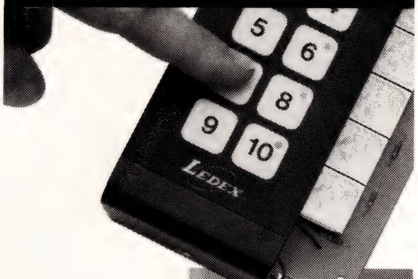
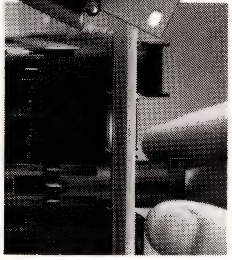
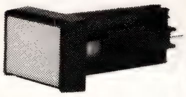
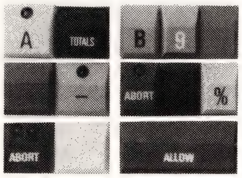
CIRCLE NO 101

3 new panel switches and pushbuttons






Rafi Series 75



Lucas NSF Pushbuttons

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Lucas NSF Keylite® keyboard switches are noted for low cost, dependability, 5 million cycle life, and versatility.

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CIRCLE NO 21

Phone-book-size servo amp has η=98% at 4.5-kW output

According to its manufacturer, the Model 241 servo amplifier offers the industry's lowest watts-per-kilowatt power-loss figure. The servo amp uses pulse-width modulation to control the power delivered to its load. It dissipates 77W when it delivers 4.5-kW load power, so it's satisfied with air cooling, as opposed to the more costly and inconvenient water cooling needed by amplifiers having lower power efficiency.

Measuring 6.5×10.5×2.4 in., the 241 delivers ±150V at ±30A continuous and ±60A pk to motor loads. These figures correspond to 6 and 12 hp, respectively. The amplifier's 22-kHz switching frequency eliminates audible hum. This frequency also lets you use the unit to drive low-inductance motors without adding any external inductance (which could adversely affect loop response).

Accepting 24 to 165V power supplies, the 241 offers full 4-quadrant operation. For most duty cycles, you need no external heat sink. For applications that require heat sinking, the manufacturer offers a mating heat sink. The amplifier contains fail-safe circuitry that protects the unit against damage from output overloads, excessive temperature rise, and improper power-supply voltages.

An internal dc-dc converter allows you to operate the 241 from a single-ended power supply. Variable current limiting in the amplifier is adjustable from 5 to 100% of peak rated current. A smaller version, Model 240, has half the 241's power ratings: ±150V at ±15A continuous, ±30A pk. Unit prices are $990 for the 241; $650 for the 240.

—*Bill Travis*

Copley Controls Corp, 375 Elliot St, Newton, MA 02164. Phone (617) 965-2410. TLX 285957.

Circle No 729

***For most applications, you don't need a heat sink** for the Model 241 PWM servo amplifier. The unit delivers power outputs as high as 4.5 kW at 98% efficiency. Its 22-kHz switching frequency eliminates audible hum and simplifies the driving of low-inductance motors.*

Standards Update

EMISSIONS CRACKDOWN— INSIDE THE FCC

It began in August, 1985, with a one million dollar seizure at Seequa Computer, followed with a crackdown on microcomputer manufacturers (March, 1986). Then in April, the FCC swept through Comdex, levying more than $250,000 in fines. The ominous nature of these actions by the FCC to enforce its computer emissions standards has left the industry wondering "What's next?" According to the leading laboratory in the field, Dash, Straus & Goodhue, Inc., of Boxborough, Massachusetts, it will be a move by the FCC to use its own Laurel, Maryland, laboratory to test mass marketed PCs to see who's non-compliant. The full range of FCC penalties, fines, seizures and arrests, could follow. In addition, the FCC has begun checking Customs files to see if the required FCC "740" form has been included. Failure by importers to file can result in a host of Customs related penalties in addition to the FCC's.

Help is on the way, however, from Dash, Straus & Goodhue (617 263-2662), the Northeast's largest testing, research and development firm dedicated to EMI, telecom and safety compliance. Customers can call DSG and receive, over the phone, a commitment to have a device tested, modified (if necessary), retested and verified within a guaranteed time for a guaranteed rate. DSG is an NBS accredited laboratory for emissions and telecommunications testing.

Circle Reader Service No. 102 for Dash, Straus & Goodhue.

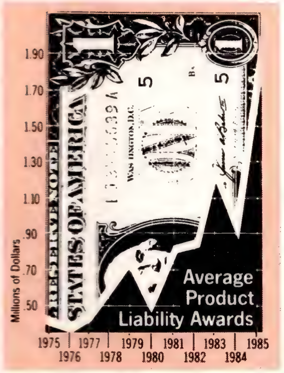
IS DDS THE NEXT TARGET FOR THE FCC?

Since it issued its Third Report and Order, Docket 81-216, in November of last year, the FCC has required nearly all manufacturers of Digital Data Systems to register their designs with the FCC. This includes Channel Service Units (CSU), Network Channel Terminating Equipment (NCTE), and nearly any device that interfaces with T1 or subrate lines. Also included are devices that encode *analog* signals, even though they interface through NCTE or CSU. Some manufacturers have been slow to comply, and their competitors have filed charges. The FCC has responded, issuing forfeitures to three manufacturers based on a complaint by Verilink.

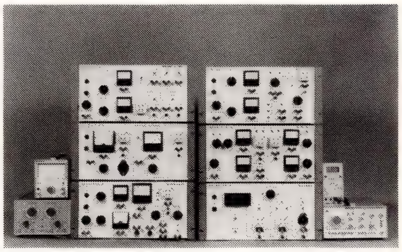
Registering equipment for DDS connection is tricky. One lab proficient in the field is Dash, Straus & Goodhue, Inc., of Boxborough, Massachusetts. As an extra plus, the firm is one of the few labs also approved by the Canadian Department of Communications and can arrange for approvals in Canada as well.

PRODUCT SAFETY— REFORM GAINS BUT LISTING IS BEST

Efforts to reform product liability laws have made slow gains in Congress. The liability Tort Reform Bill S.2760 has passed the Senate Commerce Committee 10 to 7. Basically, it encourages settlement by requiring manufacturers to make a reasonable offer in settlement prior to trial. If not accepted, the injured party's claim for pain suffering is limited to $250,000. But progress and reform is slow and sure to run into opposition in the House. The best bet to hedge against lawsuits may be UL® listing and CSA® certification. While not a complete defense, failure to meet standards could leave a manufacturer with practically no defense in cases of shock or fire hazards. These and other worldwide safety approvals can now be obtained through one company, Dash, Straus & Goodhue, Inc. DSG can design, test, and coordinate submittals of products for UL, CSA, and West German approvals, often handling them simultaneously. Final tests carried out by these organizations are coordinated through DSG.



NEW INSTRUMENTS SPEED COMPLIANCE

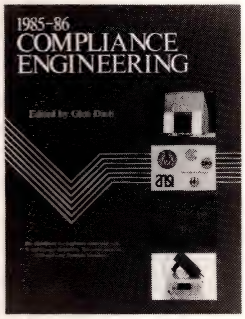


An integrated workstation designed for the complete evaluation of telephones, modems, PBXs etc. for compliance with FCC Part 68, DOC DS-03 and EIA standards is now available from Compliance Design Inc. (617 264-4668). The Workstation makes setting up Part 68 laboratories practical for those manufacturers who wish to avoid heavy independent laboratory testing fees. The Workstation has become especially popular for manufacturers since they now have to meet the FCC's requirement of a six-month recheck on all equipment previously registered.

To ensure EMI compliance, CDI also makes available the famous Roberts Antenna.® The antenna is known for its near lossless receive characteristics and is identical to those used by the FCC for 25 years. Now an industry standard, the company guarantees that any reasonable site can meet the FCC's critical site attenuation requirements of OST-55 by using these antennas. In fact, as part of a package, CDI's engineers will test any customer's site and file it with the FCC, a prerequisite to using it for EMI testing. The antenna was designed by Willmar Roberts, former Assistant Chief Engineer of the FCC's laboratory in Laurel, Maryland. It is available exclusively from Compliance Design.

Circle Reader Service No. 103 for Compliance Design Inc.

THE BEST *IS* AVAILABLE—FOR FREE!



The industry's standard handbook on EMI, ESD, telecom and safety, Compliance Engineering 1987 covers specifications and methods of engineering for Safety, EMI, ESD, and Telecom compliance. With the need to comply with these specifications universally recognized, engineers have sought out, but been unable to find, authoritative sources for issues related to designing for compliance. Now in Compliance Engineering, separate sections covering EMI, safety, telecom and ESD give a step-by-step approach to control and compliance. The 1985–86 edition drew rave reviews from its readers. You can receive the 1987 issue (available in January, 1987) free of charge just by circling the Reader Service Number below.

For *COMPLIANCE ENGINEERING 1987,* circle Reader Service No. 104.

Dash, Straus & Goodhue, Inc., 593 Massachusetts Avenue, Boxborough, MA 01719 617 263-2662

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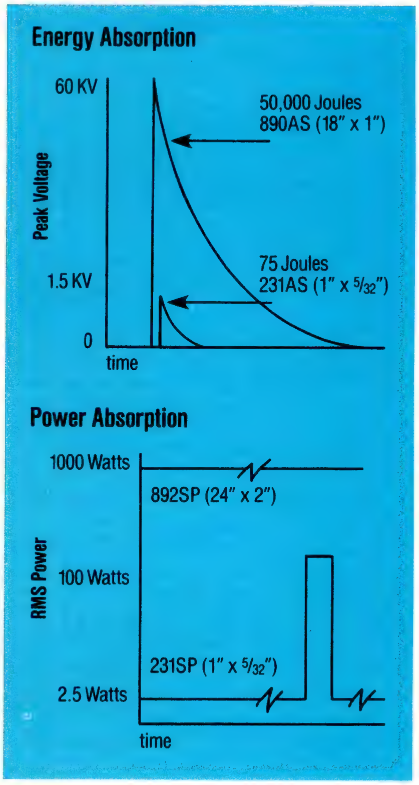

Regardless of the pulse shape, we have the resistor. Our Type SP handles large amounts of power from 60 cycles through VHF. Type AS can absorb huge amounts of energy in millisecond pulses. Type A solves high resistance problems in high voltage situations.

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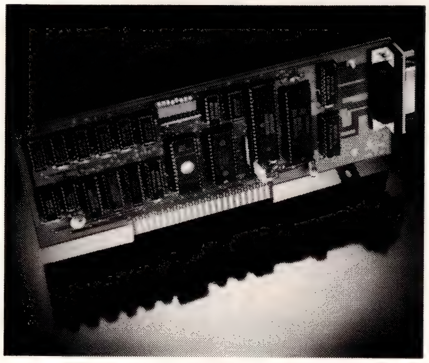
Board simplfies IEEE-488 instrument-control programs

The 500-IEEE board can simplify the programming needed to control as many as 14 IEEE-488 instruments. Sporting its own microprocessor, the board integrates high-level IEEE-488 control in single-line commands, making programs easy to read and write.

Instead of plugging the 500-IEEE board into a slot in your IBM PC or compatible computer, you plug it into the manufacturer's Series 500 scientific or System 570 data-acquisition workstation. This configuration frees your PC for other tasks and concentrates instrument control in a single intelligent workstation.



Offering a simplified programming environment *for low-cost IEEE-488 instrument control, the 500-IEEE board plugs into the manufacturer's Series 500 or System 570 workstations, freeing your personal computer for other tasks.*

The 500-IEEE card operates as an intelligent IEEE-488 multicontroller with a command set that provides a complete selection of IEEE-488 capabilities. You can use the board to implement serial and parallel polling; provide low-level bus control; and handle the input and output of strings, numeric data, and arrays. The unit's software-programmable terminators make it compatible with all IEEE-488 instruments.

The board converts the high-level Soft500 measurement and control commands used by the Series 500 and System 570 workstations into English-like instructions for bus activities. These commands are similar to those used by Hewlett-Packard's Series 80 IEEE-488 bus controllers.

The degree to which the 500-IEEE board simplifies programming is evident when you compare a program for the 500-IEEE with a program (in National Instrument's Plus 500 programming language) for one of the manufacturer's earlier IEEE-488 cards. For example, a 13-line program for the 500-IEEE offers the same functionality as that of a 31-line Plus 500 program. The 500-IEEE program sets up the bus in a known state with the command: PRINT #1, "ABORTIO". In Plus 500, the same command requires six lines of cryptic code.

In conjunction with the manufacturer's Series 500 or System 570 workstations, the board provides the function of a multicontroller at low cost. For example, at $2295, a System 570 workstation with a 500-IEEE board and a 16-relay power control would allow 31.2 memory-mapped readings/sec for 32 single-ended analog inputs, 16 differential analog inputs, or 16 TTL digital inputs. Such a system would also let you run such programs as LabTech, Asyst, and Asystant+. A similarly configured HP 6942-A multiprogrammer can perform 18,000 readings/sec, but costs three times as much. The 500-IEEE alone costs $650.—***J D Mosley***

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400. TLX 985469.

Circle No 725

CIRCLE NO 22

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The bottom line?

More capability in less space. Faster setup. Less cabling. *And* low cost of ownership at all stages of system development.

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Put us on the rack starting today...all models are in stock now! For more information and our DC Power Supply Catalog, contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

DESIGNED FOR HP-IB SYSTEMS

HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

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CIRCLE NO 105

EI15617

For winning 8051 family designs that meet your time-to-market deadline and engineering budget—you'll need development tools, particularly In-Circuit Emulation.

The price of your success? From $1,500 to $5,000 with MetaLink's PC-hosted 8051-family of development tools and add-ons!

With our MetaICE-52 tool for example, you can add real time, transparent 8052-family In-Circuit Emulation to your lab PC for $3,295—a fraction of the cost of large, dedicated development stations.

All MetaICE units plug in to your IBM or compatible PC via a standard RS-232 serial port. In one compact box, you get full symbolic debug, 16,000 hardware break points, 16K of both program and external data memories, 12 break conditions, all microcontroller modes supported—and much more.

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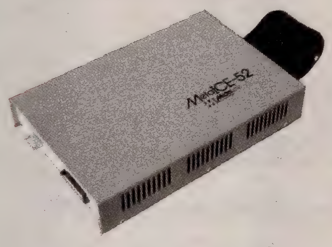
All MetaICE units are affordable—like our $2,895 MetaICE-51 for 8051 emulation, the MetaICE-31 for 8031 support ($1,495) and our 80515 unit, the MetaICE-80515, just $4,995.

MetaICE units are available for the full range of 8051 family devices:



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CIRCLE NO 106

User-configurable STD Bus memory card combines 1M byte of EPROM and RAM

If your STD Bus-based system requires a mixture of EPROM and RAM cards, you may, depending on the constraints of your design, be able to reduce your board count by taking advantage of the SB8122 memory card's memory-mixing capability. The universal memory board can hold 8k bytes to 1M byte of a combination of EPROM and RAM.

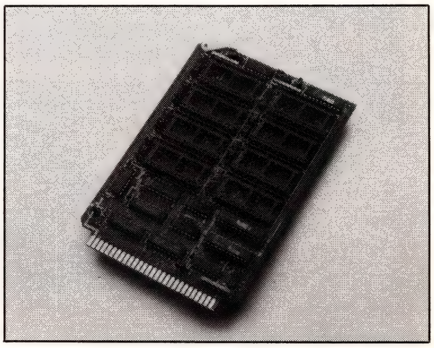
The board uses relatively expensive static RAMs (which spec a 250-nsec access time) instead of cheaper dynamic RAMs, because the static RAMs don't require refresh signals and can work with zero wait states. In a dynamic-RAM-based memory board, the refresh signal is generated from the bus clock line, and this signal can conflict with the STD Bus's DMA signals. Remember also that if your system requires a mixture of RAM and EPROM, the cost savings of eliminating a second memory board can offset the 40 to 50% price premium for the static RAMs.

The memory's address-decoding circuitry is PLD-based; you can either choose from the board's standard set of memory maps via jumpers, or you can create your own PLD decoder. If they're needed, you can insert wait states by installing jumpers.

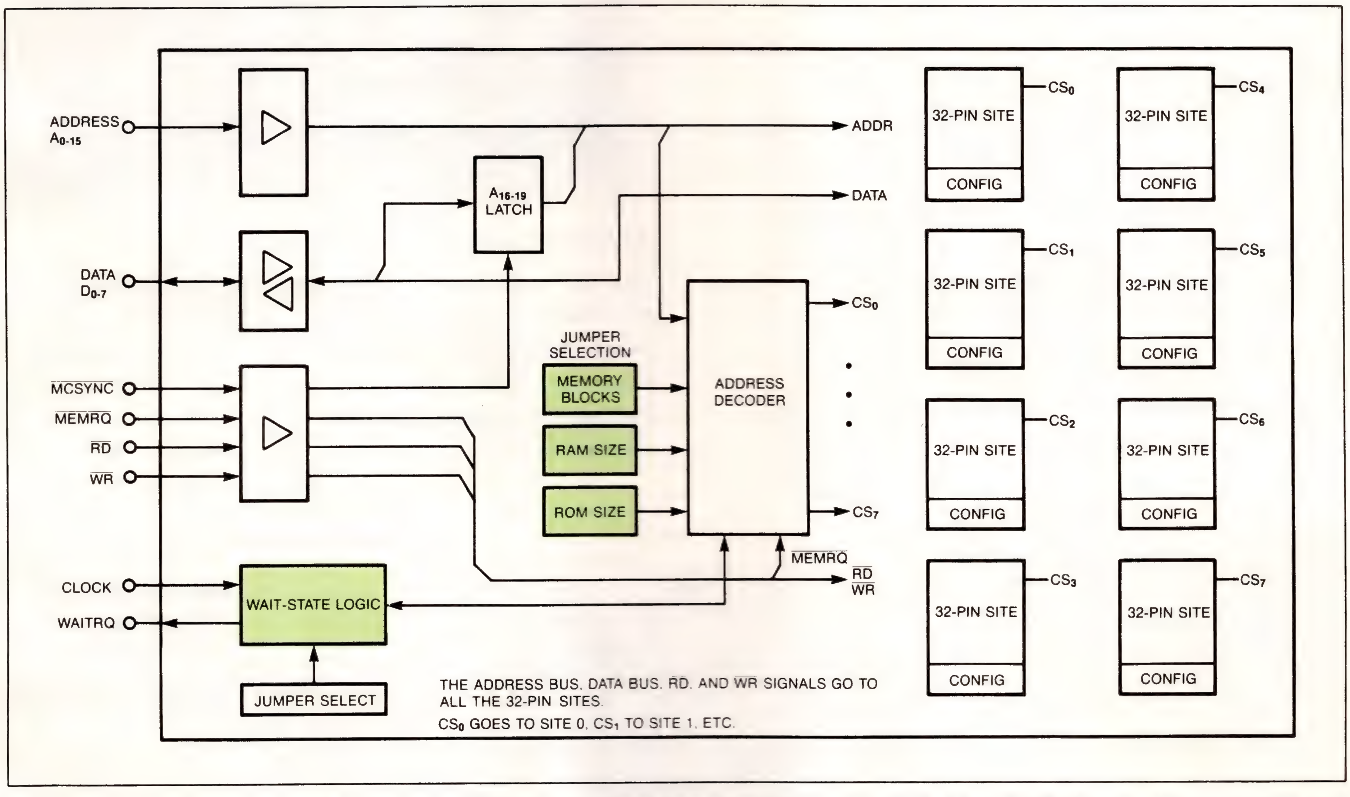
The board has eight 32-pin JEDEC sockets, which are upwardly compatible with 28-pin devices. Unpopulated, the SB8122 costs \$145; with 512k bytes of static RAM, \$595.—***Margery S Conner***

Micro/sys, 1011 Grand Central Ave, Glendale, CA 91201. Phone (818) 244-2600.

Circle No 726



This universal memory card can hold 8k bytes to 1M byte *of a combination of EPROM and static RAM. The SB8122 supports the 2764, 27128, 27256, 27512, and 27010 EPROMs, among others. The 250-nsec static RAM can be organized as 8k×8, 32k×8, or 128k×8 bits.*



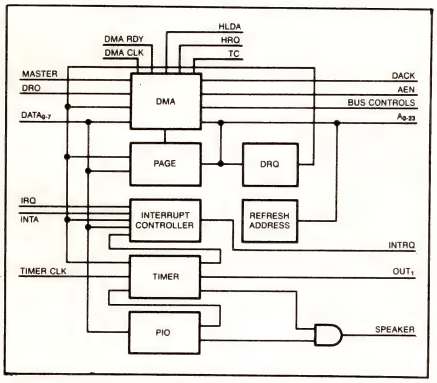
You configure, via jumpers, each socket *on the SB8122 by memory type. Jumpers also select RAM and EPROM size and the number of wait states.*

READERS' CHOICE

Of all the new products covered in EDN's **November 27, 1986**, issue, the ones reprinted here generated the most reader requests for additional information. In case you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **November 27, 1986**, issue.

SCHEMATIC EDITOR

The Hiwire schematic-drawing package extracts symbols from a library of 700 components and connects the components with wires and buses (pg 245).
Wintek Corp.
Circle No 602

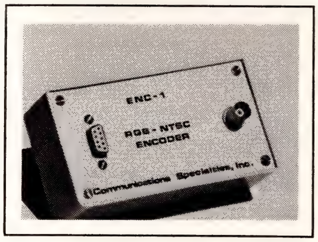


CONTROLLER CHIP

The FE3010A peripheral-controller chip, when coupled with the FE3000 CPU-controller IC, implements an IBM PC/AT in only 4.5×7 in. of board space (pg 92).
Faraday Electronics Inc.
Circle No 601

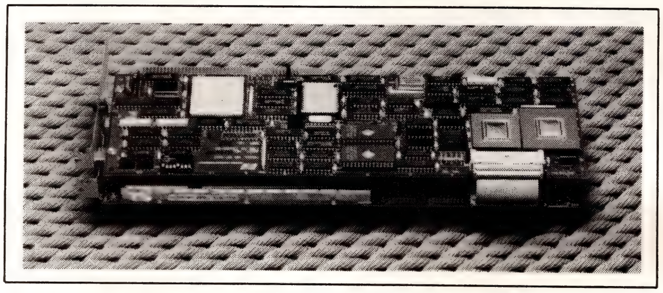
VIDEO ENCODER

The Model ENC-1 is a composite video encoder for converting standard analog RGB and synchronous color-video signals to standard NTSC composite video signals (pg 252).
Communications Specialties Inc.
Circle No 604



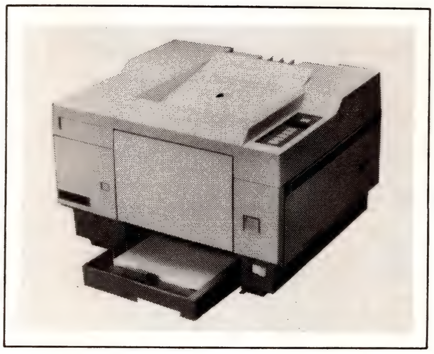
FILM RECORDER

The CompactColor Model 635 produces digital images of 16- and 35-mm movie frames (pg 258).
Dunn Instruments.
Circle No 606



MAP INTERFACE

The MP-500 board set supports the manufacturing automation protocol (MAP). It plugs into the backplane of an IBM PC/XT, PC/AT, or compatible computer (pg 256).
Industrial Networking Inc.
Circle No 605



LASER PRINTER

The L1012 prints at 12 pages/minute and provides 300×300-dots/in. resolution. It lets the operator perform all maintenance (pg 250).
Printronix Inc.
Circle No 603

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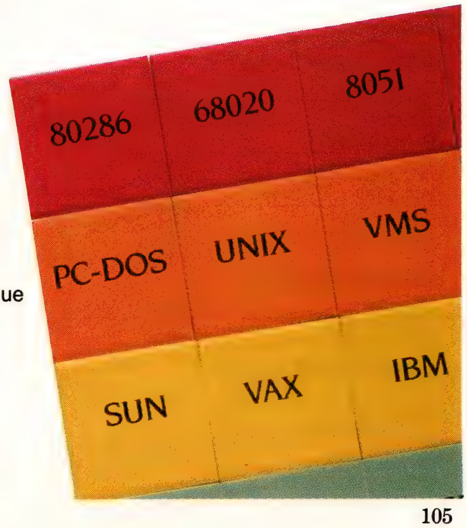

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CIRCLE NO 107

LEADTIME INDEX

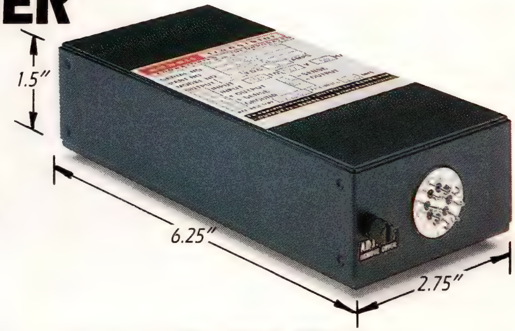
Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	25	59	8	8	0	8.8	8.1
Pot-Core	0	13	63	12	12	0	10.5	8.2
Laminate (power)	0	28	61	5	6	0	8.0	7.7
CONNECTORS								
Military panel	11	22	45	11	11	0	8.8	9.6
Flat/Cable	23	41	23	9	0	4	5.9	3.9
Multipin circular	0	21	43	36	0	0	9.6	8.9
PC	11	45	33	11	0	0	5.7	6.0
RF/Coaxial	17	50	17	16	0	0	5.4	4.4
Socket	23	53	12	12	0	0	4.4	4.7
Terminal blocks	12	47	29	12	0	0	5.6	4.2
Edge card	9	41	32	14	4	0	7.0	5.5
Subminiature	18	41	23	12	6	0	6.4	6.5
Rack & panel	10	50	20	20	0	0	6.2	5.8
Power	8	23	54	15	0	0	7.4	5.7
PRINTED CIRCUIT BOARDS								
Single-sided	0	65	35	0	0	0	4.8	5.4
Double-sided	0	30	70	0	0	0	6.5	4.3
Multilayer	0	18	65	13	4	0	8.9	7.2
Prototype	0	79	16	5	0	0	4.4	2.7
RESISTORS								
Carbon film	37	33	19	11	0	0	4.2	3.1
Carbon composition	35	38	19	8	0	0	3.9	5.4
Metal film	33	29	29	9	0	0	4.5	3.8
Metal oxide	25	33	42	0	0	0	4.3	5.6
Wirewound	43	43	14	0	0	0	2.4	6.4
Potentiometers	19	33	33	15	0	0	5.9	6.6
Networks	19	29	38	14	0	0	6.1	5.6
FUSES	43	43	14	0	0	0	2.4	3.0
SWITCHES								
Pushbutton	26	44	17	13	0	0	4.7	4.9
Rotary	10	45	35	10	0	0	5.7	5.3
Rocker	26	42	21	11	0	0	4.6	5.0
Thumbwheel	20	40	27	13	0	0	5.4	7.5
Snap action	36	46	9	9	0	0	3.5	4.5
Momentary	37	27	27	9	0	0	4.4	5.4
Dual in-line	20	60	10	10	0	0	4.2	5.5
WIRE AND CABLE								
Coaxial	50	44	6	0	0	0	1.8	3.6
Flat ribbon	59	32	9	0	0	0	1.7	3.6
Multiconductor	47	35	12	6	0	0	2.9	4.0
Hookup	58	38	4	0	0	0	1.5	1.7
Wire wrap	67	33	0	0	0	0	1.0	2.8
Power cords	20	48	28	4	0	0	4.3	4.4
Other	33	17	33	17	0	0	5.8	3.2
POWER SUPPLIES								
Switching	10	37	37	16	0	0	6.5	9.0
Linear	17	50	25	8	0	0	4.8	8.1
CIRCUIT BREAKERS	22	28	39	11	0	0	5.7	6.6
HEAT SINKS	35	35	24	6	0	0	3.9	4.3

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	32	21	37	10	0	0	5.2	6.5
PC board	10	32	32	21	5	0	8.1	8.3
Dry reed	8	33	42	17	0	0	6.9	10.0
Mercury	0	29	57	14	0	0	7.6	11.0
Solid state	8	31	31	23	7	0	8.9	8.2
DISCRETE SEMICONDUCTORS								
Diode	39	18	39	0	0	4	4.8	4.5
Zener	39	9	35	17	0	0	5.7	4.9
Thyristor	27	7	53	13	0	0	6.5	6.4
Small signal transistor	35	20	30	15	0	0	5.3	7.1
FET, MOS	13	20	53	7	7	0	7.6	7.8
Power, bipolar	15	39	46	0	0	0	4.8	4.5
INTEGRATED CIRCUITS, DIGITAL								
CMOS	23	31	27	15	4	0	6.4	7.6
TTL	26	22	39	9	0	4	6.5	4.7
LS	32	18	39	7	4	0	5.7	5.0
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	25	12	50	13	0	0	6.3	7.9
OP amplifier	10	37	37	16	0	0	6.5	8.0
Voltage regulator	14	33	34	19	0	0	6.6	6.8
MEMORY CIRCUITS								
RAM 16k	14	57	29	0	0	0	4.0	8.4
RAM 64k	17	50	33	0	0	0	4.2	6.7
RAM 256k	18	46	27	19	0	0	5.0	7.7
ROM/PROM	0	55	45	0	0	0	5.3	8.0
EPROM	14	41	27	14	0	4	6.9	7.3
EEPROM	8	31	46	8	0	7	8.2	8.3
DISPLAYS								
Panel meters	9	46	27	18	0	0	6.4	5.7
Fluorescent	0	29	43	14	14	0	10.1	10.0
Incandescent	0	75	25	0	0	0	4.3	9.3
LED	9	54	23	14	0	0	5.6	5.9
Liquid crystal	0	39	46	15	0	0	7.2	8.7
MICROPROCESSOR ICs								
8-bit	20	53	20	7	0	0	4.2	7.3
16-bit	20	70	10	0	0	0	2.9	8.2
FUNCTION PACKAGES								
Amplifier	0	63	37	0	0	0	4.9	8.3
Converter, analog to digital	0	39	38	15	8	0	8.6	10.8
Converter, digital to analog	0	40	40	10	10	0	8.5	10.7
LINE FILTERS	0	50	38	12	0	0	6.4	7.5
CAPACITORS								
Ceramic	23	41	21	15	0	0	5.2	4.9
Ceramic monolithic	20	40	25	15	0	0	5.5	5.4
Ceramic disc	27	31	27	15	0	0	5.5	5.6
Film	21	24	45	10	0	0	5.9	6.7
Electrolytic	19	37	18	26	0	0	6.6	6.3
Tantalum	15	37	26	22	0	0	6.6	7.2
INDUCTORS	8	38	54	0	0	0	5.5	8.6

Source: *Electronics Purchasing* magazine's survey of buyers

ABBOTT'S NEW M25; A HIGHER PERFORMANCE, 25-WATT SWITCHING POWER SUPPLY



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MODEL M25 SPECIFICATIONS

DIMENSIONS	**6.25″x 2.75″x 1.5″**
Input frequency	*47-440 Hz*
Input voltage	*103.5 to 126.5 V rms*
Outputs	*5, 12, 15, 24, 28 V*
Efficiency	*70% minimum*
Ripple/noise	*20 mV rms/100 mV p-p*
Line regulation	*10 mV*
Load regulation	*25 mV*
EMI	*MIL-STD-461B*
Environment	*MIL-STD-810C* *MIL-S-901C*
Input protection	*MIL-STD-1399 sec 103*
Operating temperature range	*– 20°C to 71°C*
Storage temperature range	*– 55°C to 85°C*
MTBF (ground benign)*	
Standard	*176,000 hours*
ER Option	*759,000 hours*
MTBF (naval sheltered)*	
Standard	*33,000 hours*
ER Option	*125,000 hours*

**MIL-STD-217D (50°C baseplate)*

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MILITARY POWER SUPPLIES

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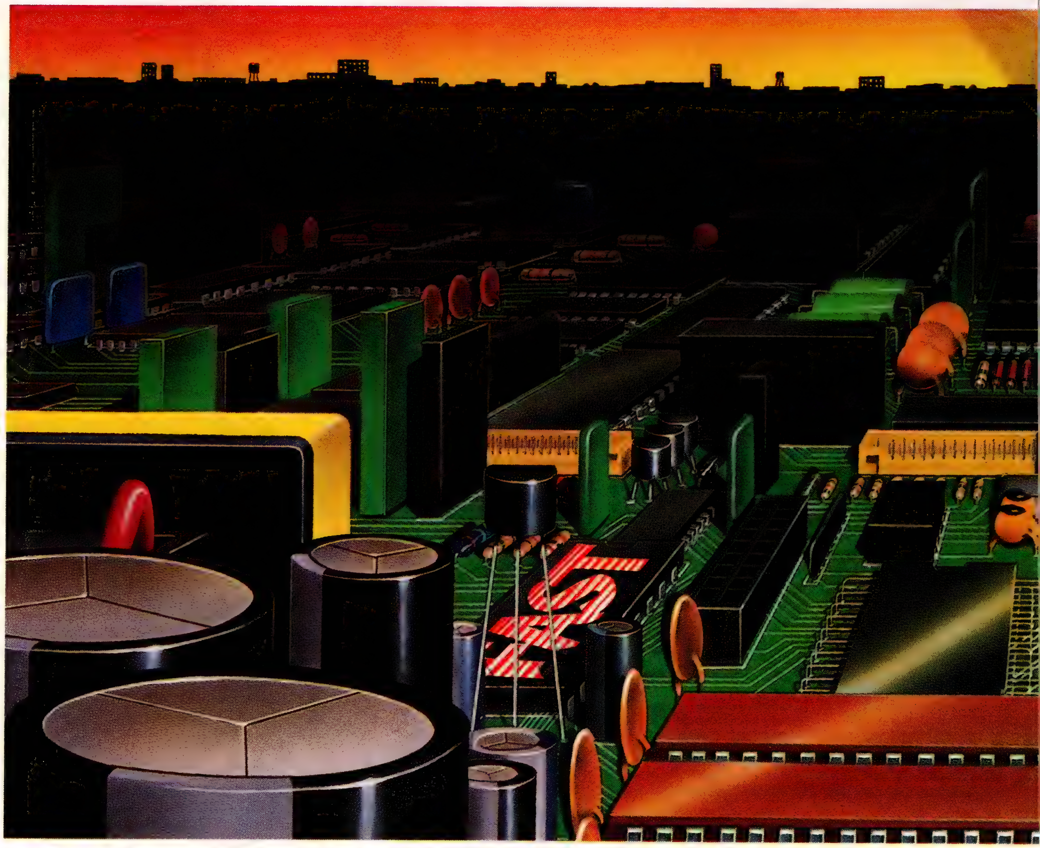

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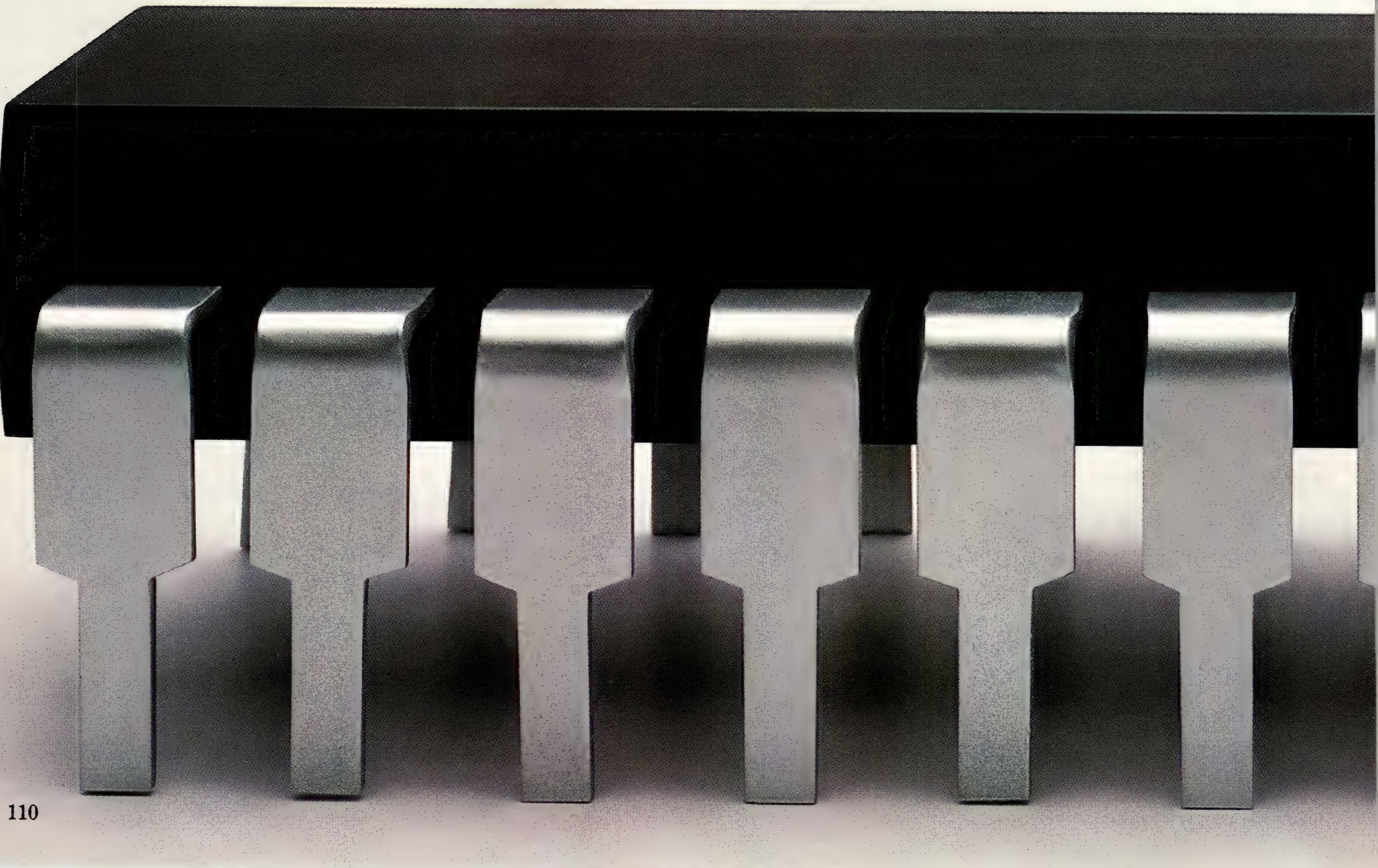

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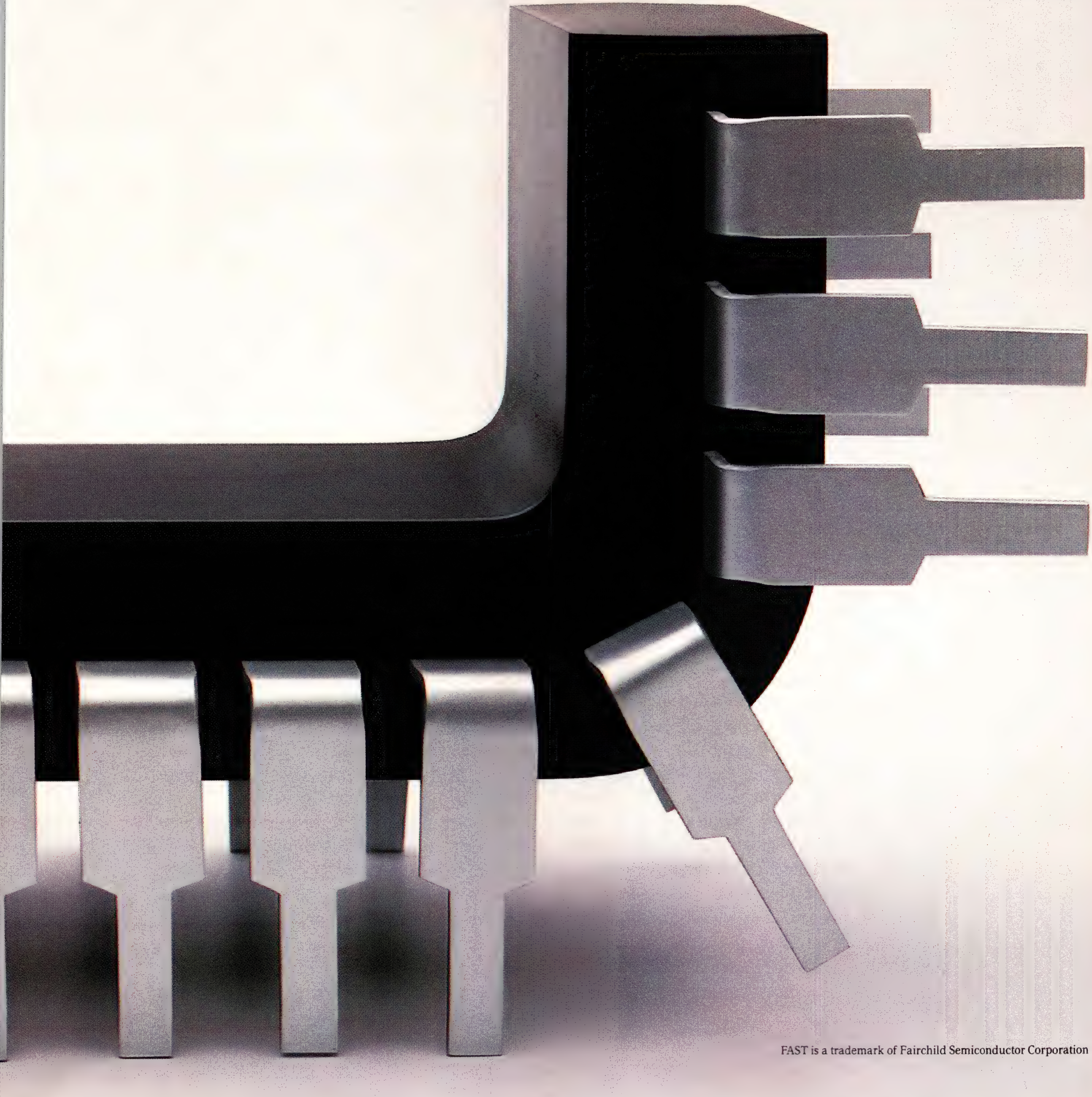

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Special Report

Programmable-logic devices

Charles H Small, *Associate Editor*

The news from the programmable-logic-device (PLD) front is nothing but good. Conventional PLDs with a programmable-AND/fixed-OR array (engineers refer to such devices generically as PALs—a Monolithic Memories trademark) are benefiting from a host of improvements: New process technologies and architectural enhancements are making the devices faster and more flexible.

Meanwhile, a collection of new, very large programmable devices is challenging gate arrays for lower-end ASIC applications. These large PLDs offer the same advantage over 20- and 24-pin PLDs as the smaller PLDs do over SSI and MSI devices: One 20- or 24-pin PLD can replace a handful of SSI and MSI devices, and one large PLD can replace 10 to 15 of the 20- and 24-pin PLDs.

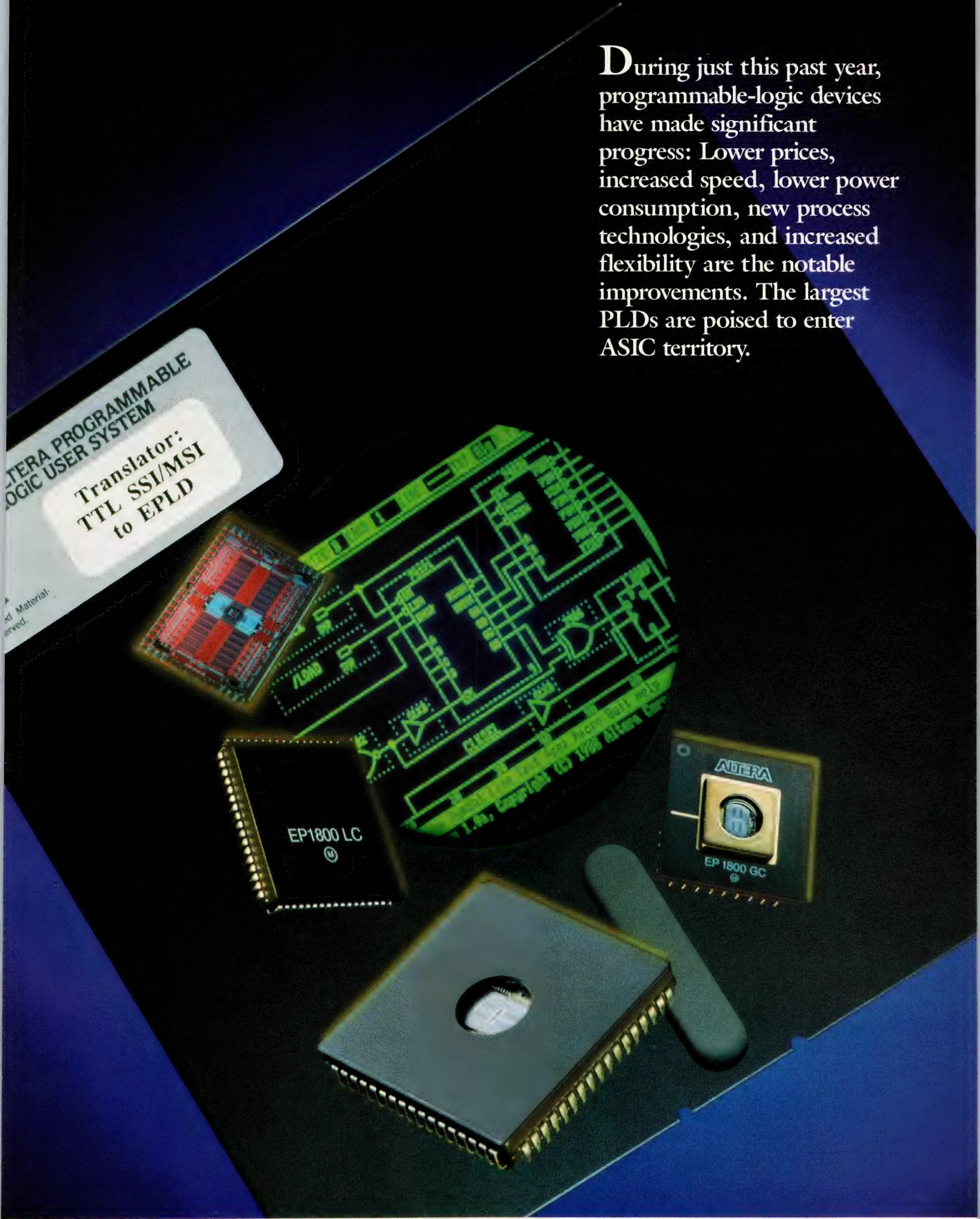
New processes and improvements in existing technologies have had a major impact on conventional 20- and 24-pin PLDs. A glance at **Table 1** (page 128) shows that PLDs come in virtually every process technology imaginable except gallium arsenide. You can obtain bipolar-TTL PLDs in four speed grades (standard, A, B, and D), plus ½- and ¼-power versions. PLDs are also now fabricated in ECL, CMOS, and zero-standby-current CMOS. Furthermore, programming methods encompass several types of metal and silicon fusable links, EPROM links, EEPROM links, and static-RAM links.

PLD makers, however, aren't much help in making sense of this welter of devices. The PLD makers spew forth a torrent of "advantages" for their particular products, but surprisingly few of these features affect the most important part of a design engineer's job—designing. Most of the so-called advantages touted by the PLD makers are of peripheral interest, or just plain no interest, to designers.

Take, for example, the security fuse that keeps a rival company from reading out the fuse map of your programmed PLD—good news for company management, but little help to an engineer slaving over a logic design. Similarly, as PLD applications expand to include more state-machine designs, in addition to the usual combinatorial functions such as address decoders, the preset and clear inputs of newer PLDs become very important to test engineers—but again, not to designers. To be sure, without preset and clear lines, the test engineer has a difficult time initializing a state machine to a known state, and being able to do so can shorten test times considerably.

Test engineers have accrued other benefits from recent developments. Makers of erasable devices point out, quite rightly, that their products are 100% testable before programming, whereas fuse-programmable parts are not. Complete testability and the resulting higher programming yields are good news to the

During just this past year, programmable-logic devices have made significant progress: Lower prices, increased speed, lower power consumption, new process technologies, and increased flexibility are the notable improvements. The largest PLDs are poised to enter ASIC territory.



Today's PLDs achieve complexities that derive from software-aided design techniques. (Photo courtesy Altera Corp)

New, very large PLDs are challenging gate arrays for lower-end ASIC applications.

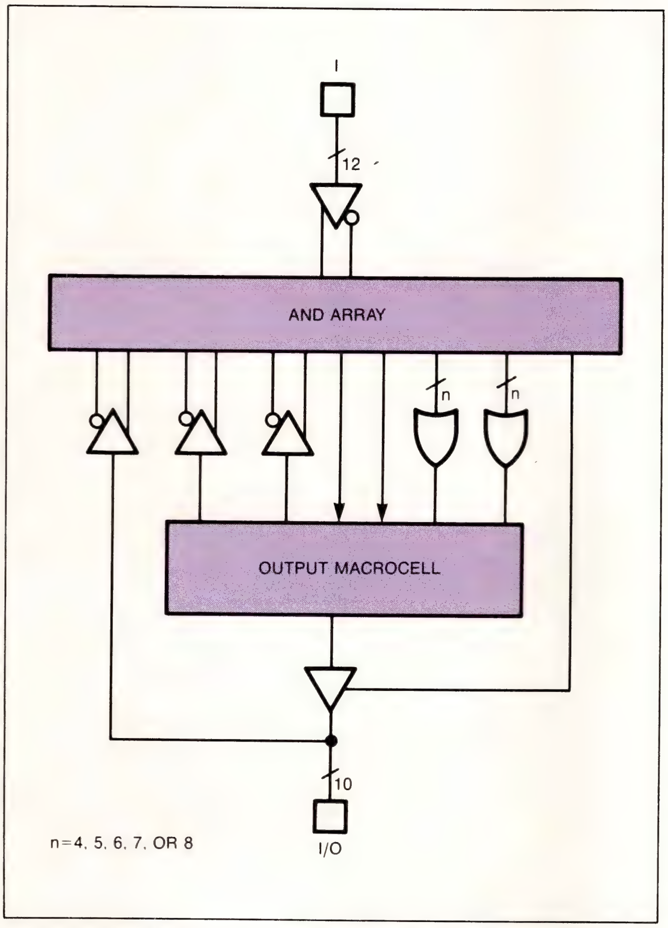


Fig 1—Resembling an enriched 22V10, *the Amtel V750 has two flip-flops and two OR gates per output macrocell. Multiplexers in the macrocell allow you to feed back—or "bury"—both OR gates' outputs as well as the outputs of both flip-flops.*

test department and the production manager, but they don't increase designers' options. Makers of erasable devices further cloud the issue with competing claims about which technology is easiest to test, which comes in the cheapest package, and which has the smallest die size.

Similarly, makers of fusable-link PLDs each tout the advantages of their various fuse technologies. You can choose from a number of metal and silicon types. The determining factor for choosing one fuse type over another is programming yield. But the lost time and extra costs incurred because of devices that don't program properly come out of manufacturing's budget, not design's.

Electrically erasable devices are easier to test—their greatest advantage. UV-erasable devices require additional test circuitry. Note also that EEPLDs come in plastic packages, while the only EPLDs available in plastic packages are one-time-programmable devices. But whichever technology you choose—erasable or fusable-linked—all current PLDs, except one, still allow only "blow and go" development methods for the design engineer. Only Xilinx has an in-circuit emulator for its devices.

All IC makers like to boast about how small their dies are and how efficient their process technology is. The design engineer might hope that smaller dies and high manufacturing yields for the IC makers would result in lower prices for the IC user, but it's competitors' prices, and not the cost of manufacture, that are the major determining factor of IC prices.

Easier jobs all around

Some devices with enhanced, more flexible architectures can replace any of a larger number of older devices. Cutting the number of different devices in stock will gladden the hearts of the purchasing and materials departments, but again, it won't do much for the designer. These more flexible devices can also make the pc-board designer's job easier by allowing him to distribute combinatorial and registered outputs among different sets of pins. Such a redistribution could untangle a knotty pc-board layout problem.

The design engineer also has to wade through a welter of device characteristics that might be a factor in certain specialized applications but are of little importance to most applications. For example, take the battle of the specs between CMOS and TTL. At moderate clock rates, CMOS PLDs consume less power than do TTL PLDs. You can also get CMOS PLDs that consume virtually no quiescent power. Most designers, however, want to run their PLDs as fast as possible. At high clock speeds, CMOS and TTL PLDs consume virtually the same amount of power.

Furthermore, the new D versions of TTL PLDs exhibit 10-nsec propagation delays vs 15-nsec delays for the fastest CMOS parts. And IC makers claim that they can squeeze out one more speed upgrade from TTL technology. Don't take speed claims for PLDs at face value, however. Not all makers spec speed in the same way. Check each device's spec sheet to see if the spec holds true over the device's full temperature and supply-voltage ranges or is measured at 25°C with the optimal V_{CC}.

Finally, although CMOS tolerates noise and voltage variations from power supplies and has a better noise margin than TTL technology can provide, high-output-drive CMOS circuits (20-mA I_{OL}) can cause glitches in a system by overdriving—or "bouncing"—the system's ground.

A design engineer can filter out irrelevant specs by focusing on the three primary concerns for designing with PLDs: Can the designer get real devices that meet specs at a reasonable cost? Will the design run fast enough? Does the designer have the skills and sufficient understanding of a particular type of PLD to execute a workable design efficiently and elegantly?

Table 1 shows the speed and cost of available devices. Note that most companies listed make conventional 20- and 24-pin AND-OR PLDs. Note also that, with some exceptions, the companies that make PLDs with unusual architectures or exotic process technologies are recent start-ups. Some of the start-ups now have alternate-sourcing agreements with larger companies. Monolithic Memories and Xilinx have inked such a pact, as have Intel and Altera, and Exar has bought Exel.

However interesting the new, large PLDs and their exotic architectures may be, engineers' loudest demands have simply been for faster PLDs. Monolithic Memories has been the first PLD maker to respond with 10-nsec D versions of 20-pin PLDs. Expect other established IC makers to follow suit soon.

Just around the corner

AMD will offer ½- and ¼-power versions of its B devices this year. It will also offer some new 24-pin parts, such as a 15-nsec 20L8 and 20-nsec X-OR PLDs.

Fairchild has expanded its line of conventional 20-pin PLDs as part of its Fast logic family. The company has both 25-nsec A parts and 15-nsec B parts, including registered and programmable-output-polarity devices. Similarly, Texas Instruments has expanded its line of PLDs to include a series of 24-pin 20XX and 19XX parts, available in 15-, 20-, and 25-nsec versions. TI also has 35- and 25-nsec versions of the industry-standard 22V10.

Signetics has a new field-programmable logic sequencer (FLPS), the PLS179, which is a 24-pin, 18-MHz version of the PLS159. The FPLS's extension to a 24-pin device mirrors the extension of the 20-pin PLS153 FPLA (field-programmable logic array) to the 24-pin PLS173 FPLA.

The 24-pin FPLS can do the same jobs as 20R8 and 20X8 PLDs, but it has a more flexible internal architecture. Where the PLDs have a fixed-OR structure that connects eight terms to each register, the FPLS (like the FPLA) has a programmable-OR array. This array allows product-term sharing along with the ability to connect a variable number of product terms to each output. In addition, the FPLS has a buried feedback line that returns the complement of a product term to the device's AND array. The complement line simplifies certain logic expressions.

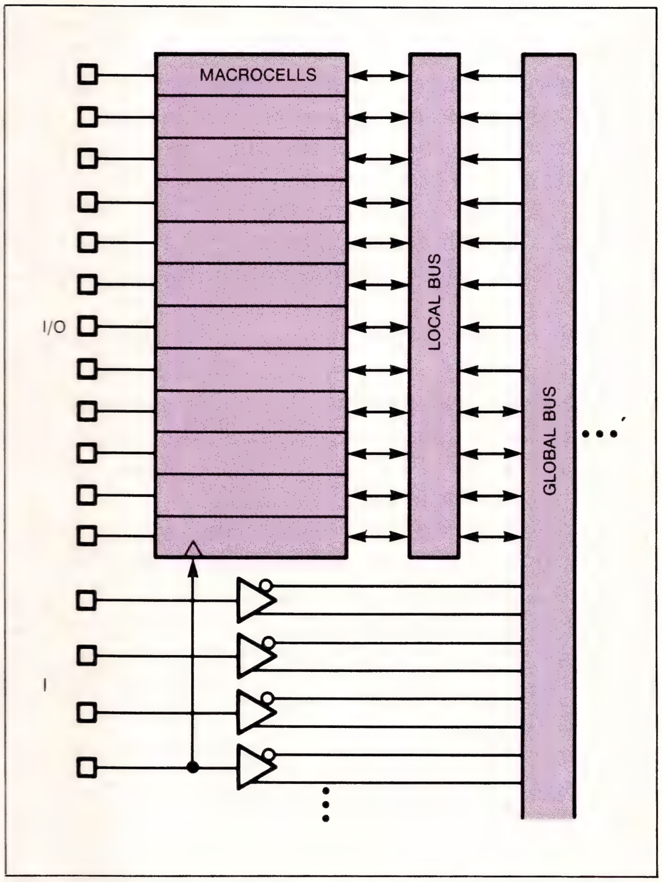


Fig 2—The largest available device with a conventional PLD architecture, *the Altera EP 1800 internally resembles four PLDs. This figure shows one quadrant of the device. Each quadrant has 12 I/O macrocells. Each quadrant's macrocells include four high-speed, four local-feedback, and four global-feedback cells. The chip also has 16 dedicated inputs.*

Extending its line of traditional 28-pin FPLSs, Signetics has introduced the PLUS405A. The device consumes 100 mW and can clock at 40 MHz. It's a superset of the older, much slower PLS105.

If the fastest TTL PLDs still aren't fast enough for your application, perhaps you need an ECL PLD. Along with National Semiconductor, Advanced Micro Devices now has ECL PLDs. For example, AMD's AmPAL20EV8 is an ECL PLD that's similar to the 22V10. The chip is available in two versions: The AmPAL20EV8 has 22V10-like outputs that you can

One 20- or 24-pin PLD can replace a handful of SSI and MSI devices, and one large PLD can replace 10 to 15 of the 20- and 24-pin PLDs.

program to be either registered or combinatorial; the second version, the AmPAL20EG8, has a slightly different output macrocell. Each output of the AmPAL-20EV8 can be either latched or combinatorial. Both 10KH and 100K versions of the chips are available.

TTL and ECL aren't the only technologies showing progress on the PLD front. Various CMOS parts are getting faster or lower in power, and the denser circuits possible with CMOS are leading to enhanced architectures.

Cypress Semiconductor now has MIL-spec, 20-pin, CMOS PLDs, for example. The UV-erasable devices have 20-nsec propagation delays. The company also makes a 25-nsec military 22V10. Last, the company has added a ¼-power PLDC20G10 that meets all of the speed specs of 24-pin TTL A parts.

The Altera EP320 is a zero-standby-power, 20-pin, UV-erasable PLD that can emulate 35- and 25-nsec, 20-pin PAL devices. Panatech, the US marketing arm of Ricoh (the only Japanese company making PLDs), has added to its line of 55- and 35-nsec, 20-pin, UV-erasable PLDs. The new addition is a 35-nsec version of the 24-pin 22V10.

Lattice's 20- and 24-pin so-called GALs (generic array logic) can substitute for most TTL 20- and 24-pin A and B devices because the company now has 15-nsec versions of its 16V8 and 20V8 electrically erasable PLDs. The company has also added an in-circuit-programming feature to its 20-pin PLDs. The 16Z8 is a 20-pin PLD in a 24-pin package; the extra four pins allow you to reprogram the device in circuit—an attractive feature, because most pc boards will undergo modifications and revisions during their manufacturing lifetime.

In addition to speed and power-consumption improvements, conventional PLDs are benefiting from a number of detail improvements and enhancements to their architectures. These enhancements typically do not require that a design engineer learn any new skills. In most cases, the enhancements simplify, rather than complicate, the design process.

For example, a device with programmable-output macrocells can emulate the output configuration of most standard combinatorial and registered PLDs. You can also set up the programmable-output device in configurations not available as conventional PLDs—for example, a 16R1, a 20R7, or even a 13L5. The added flexibility of having exactly the mix of registered and combinatorial outputs needed for a particular application is an obvious advantage for designers.

The 22V10's structure shows the extensions and refinements that PLDs have undergone. It has 132 product terms, which feed into output macrocells. You can program each of these macrocells individually to operate in one of four modes—registered or combinatorial, with either active-high or active-low polarity. In addition to offering programmable output macrocells, the 22V10 also allows a variable distribution of product terms. You can hook eight or 16 terms to a given output. Consequently, the 22V10 can be a pin-for-pin replacement for virtually all 24-pin PLDs.

Added pins and product terms

AMD's AmPAL18P8 is another example of an enhanced PLD. Compared with the earlier 16XX devices, this 20-pin device has two additional, bidirectional I/O pins and additional product terms. Signetics also has a 20-nsec version of this part.

Amtel has taken an interesting approach to expanding the architecture of the 24-pin PLD. In addition to a version of the 22V10, the company offers an enhanced device, the V750 (**Fig 1** on page 114). The V750 has much the same I/O structure as a 22V10; it has 10 selectable I/O pins and 12 dedicated input pins, while a 22V10 has 10 I/O pins, 11 inputs, and one clock pin. (Both Amtel chips are UV-erasable, CMOS parts.)

Internally, however, the V750 is more complex than a 22V10. It has two flip-flops per output macrocell instead of the 22V10's one. Both flip-flops in each macrocell have their own OR gate and their own feedback lines—true and complement—into the programmable-AND matrix, along with the usual I/O-pin feedback line. And each flip-flop has its own clock line coming from the matrix. What's more, the two OR gates have their own feedback lines into the matrix.

What Amtel designers have bought with all these extra gates, flip-flops, and feedback paths is a double benefit. First, the opportunity to decouple one or both flip-flops from the macrocell's output pin frees the flip-flops to be used as buried state registers without sacrificing an I/O pin. Second, you can fold a product term back into the AND matrix—also without sacrificing an I/O pin. The company states that the V750 can substitute for 22V10s, 32V10s, and 20RA10s and that it can handle many designs that incorporate the Altera EP600.

The Gould 18CV8 is an example of how detail upgrades of the traditional PLD architecture can yield a more flexible device. The 25-nsec, CMOS device is electrically erasable. You can set up its output mac-

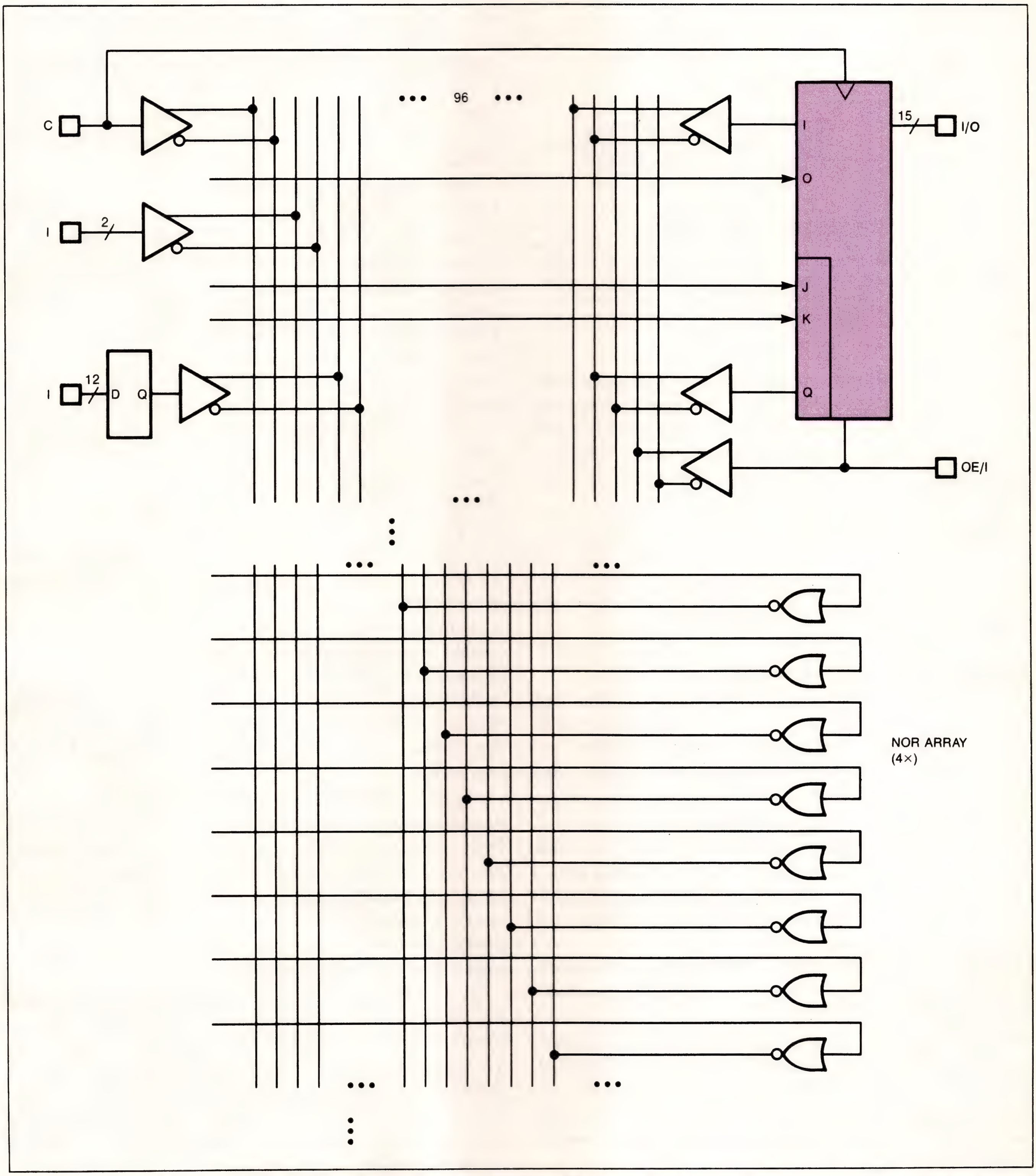


Fig 3—You might at first overlook the working heart *of the Exel 78C800. The device has a single plane of asynchronous NOR gates whose outputs feed back to their input matrix. The input and output macrocells also attach to the NOR gates' matrix.*

You can get PLDs in virtually every process technology imaginable except gallium arsenide.

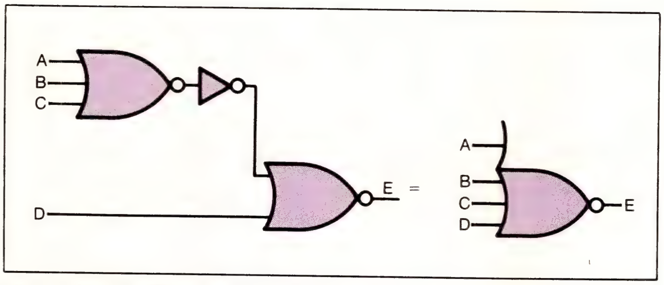


Fig 4—The 78C800 does not require the complement *of its NOR gates' output to be fed back. Consider that the asynchronous inputs can drive only NOR gates. If you inverted the output of one of the feedback terms from a NOR gate, the inverted term would, in effect, be the OR of the gate's inputs. The resulting OR's inputs could instead connect directly to the following NOR gate to achieve exactly the same logic function.*

rocells in 12 different configurations by programming bidirectional I/O pins, registered or combinatorial outputs, output polarity, and registered or combinatorial feedback into the AND-OR array. You can enable each macrocell's output independently. The device has synchronous-preset and asynchronous-clear inputs.

The device can therefore emulate most existing 25-nsec bipolar parts as well as assume more than 100 configurations not available in conventional PLDs. Gould also makes 20- and 24-pin devices that are compatible with PLS153 and PLS173 PLAs.

Buried registers yield state machine

The AmPAL23S8 is a PLD-based sequencer that combines a PLD with a classical state machine's present-state and output registers. Unlike the earlier, and much larger, 28-pin FPLS (field-programmable logic sequencer), the AmPAL23S8 is a 20-pin device. It has 14 registers and 135 product terms.

Some companies are not content to make just detail improvements to existing architectures. Much larger devices, some with entirely new architectures, now promise to shrink designs dramatically and lower system costs significantly.

Under intense pressure to shrink designs, engineers would do well to choose PLDs over semicustom devices. The large PLDs can beat small gate arrays on both device costs and nonrecurring engineering (NRE) costs like design time. The large PLDs are off-the-shelf devices that you can burn your logic design into in a matter of minutes. For gate arrays, the turnaround time from design to prototype is measured in weeks, not minutes.

PLDs have an advantage over custom and semicustom devices that's hard to measure in dollars but is nonetheless very important to engineers: Designing with PLDs generates far less anxiety in a design engineer than designing with gate arrays, because with PLDs, mistakes aren't cast in silicon. It's much easier, faster, and less costly to fix design errors and make engineering changes with PLDs than with custom devices.

The design engineer is caught here, however, on the horns of a dilemma, as he is every time he contemplates using exotic parts from new, innovative companies: If he doesn't select a new part from an innovative company, he may end up with an antiquated design that's too big and too slow; if he does select the new part, he may stumble badly while trying to assimilate a new design method. He also runs the risk of dealing with a small company that cannot provide design support, deliver workable devices, or even stay in business.

So despite the intense pressure from management to reduce the number of components in a design, engineers may continue to use the 20- and 24-pin PLDs with which they are familiar. It's easier, after all, to learn the guts of a 20- or 24-pin PLD than it is to understand the details of the new, large devices—especially those PLDs with exotic architectures that don't resemble scaled-up 20- or 24-pin PLDs.

A diagram of the internal logic of a small PLD will fit neatly on a single page of a manual; the larger, complex devices are almost incomprehensible, and their detailed logic diagrams don't fit on a single page. Consequently, the sheer size and complexity of such large devices forces designers to adopt new, computer-aided design methods.

Twenty-pin PLDs have been around long enough that experienced designers can work with them with very little in the way of design aids. An experienced designer may not even bother to write Boolean equations, instead preferring simply to mark up a diagram of a device's internal fuse map. Simple, but somewhat tedious, manual methods exist for transferring the fuse map into a device programmer.

Designers using such manual methods could justifiably question the wisdom of adopting even the least-expensive, personal-computer-based PLD software. The current generation of most PC-based, third-party software provides two classes of design support: easy-to-use, simple tricks for making somewhat annoying rote jobs easier, and ways of using non-PLD design methods to design with PLDs.

For example, transforming address ranges manually into Boolean equations is a purely rote exercise. The

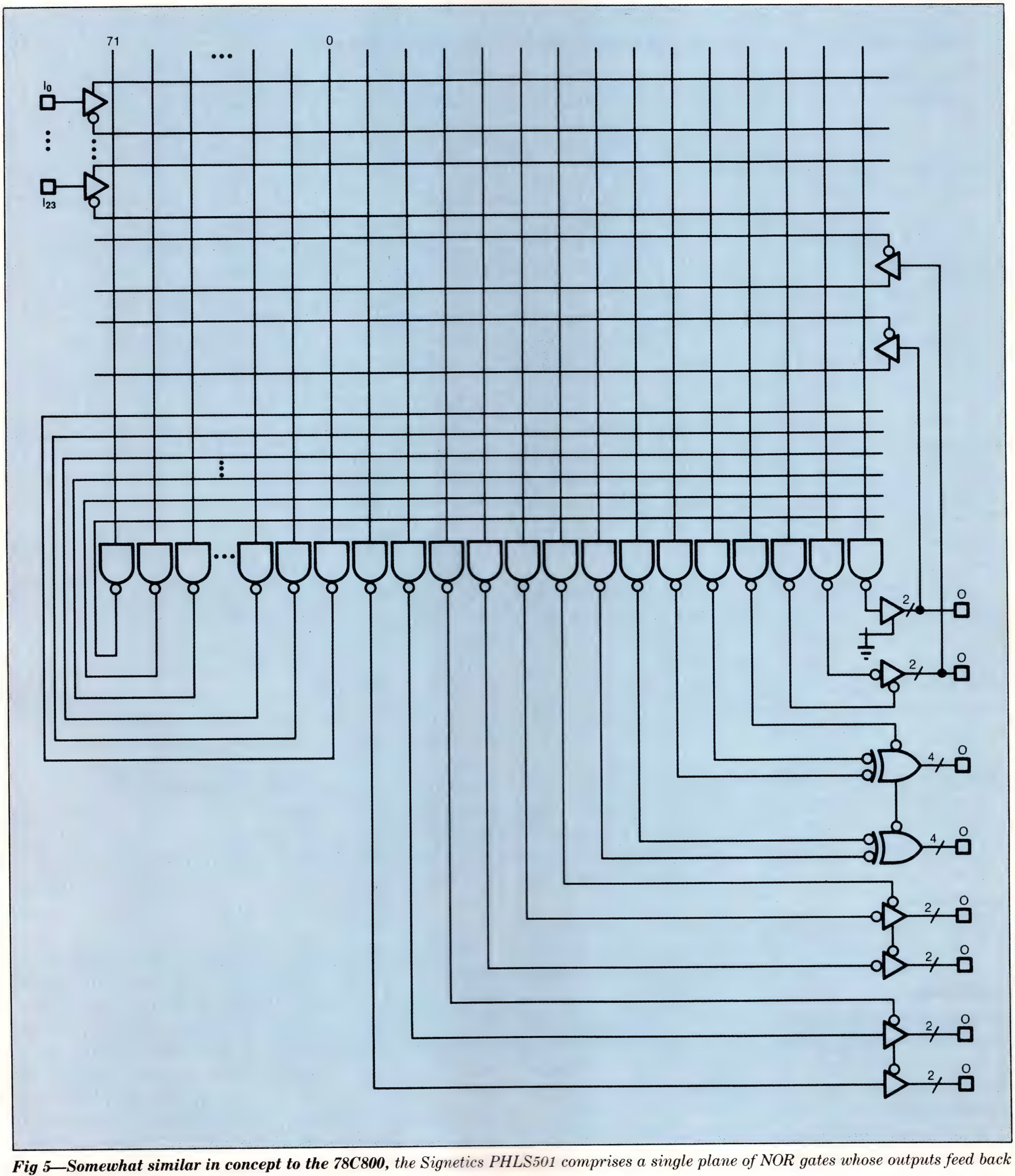


Fig 5—Somewhat similar in concept to the 78C800, *the Signetics PHLS501 comprises a single plane of NOR gates whose outputs feed back into their own input matrix.*

As PLD applications expand to include more state-machine designs, the preset and clear inputs of newer PLDs become very important in testing.

Gate equivalency approximates PLDs' relative size

The only way, presently, for a novice to get a feel for the relative size of the various PLDs is to accept the makers' data on how many 2-input AND gates their devices are equivalent to.

None of the gate equivalencies described here are absolutely accurate; all are approximations. And not all manufacturers use the same methods to arrive at their estimates.

Also keep in mind that certain applications, such as counters and shifters, use a relatively large number of registers. Such circuits can quickly use up the registers in a PLD and thereby render the remaining logic in the PLD superfluous. In short, a gate is not always a gate.

Keeping these warnings in mind, here's a selected list, in ascending order, of the equivalent gates for some PLDs:

- A 20-pin PLD=300 gates
- An Altera EP320=300 gates
- A 22V10=700 to 800 gates
- An Altera EP1210=1176 gates
- A Xilinx XC 2064=1200 gates
- An MMI MegaPAL=1500 gates
- A Signetics PML=1500 gates
- A Xilinx XC 2018=1800 gates.

only drawbacks are the time it takes to perform it and the chance for introducing human error that inevitably lurks in any manual method. In short, computerized design tools like an automated address-range feature don't enable the design engineer to do any thing he could not do before, or to think about solving his design problems in a new way.

Third-party software and some proprietary packages like Altera's A+Plus do offer (or so it seems at first) new ways to think about solving a design problem. These software packages allow you to specify a design as a state machine. Typically, you enter your design into what amounts to a for-next table as envisioned by a C programmer. (It's amusing to note the influence of C programmers on PLD software. Palasm uses standard Boolean operators familiar to engineers. Newer tools use equivalent—though occasionally bizarre looking—C operators. For example, Palasm uses a slash to represent the overbar that signifies negation; other software packages use an exclamation point for the same operator.)

These state-machine-entry programs typically employ a 2-dimensional IF structure to model a state machine. The outer, first dimension of the 2-dimensional IF statement is implied by simply listing the names of the states, one beneath the other, in a specification file. The inner IF statement is explicit in some programs and implicit in others and consists of a list of legal inputs and their corresponding outputs allowed for each state.

However exotic defining your design directly as a state machine might seem at first, these tools are a software version of manual for-next tables that engineers have used to design state machines with for years. More important, these computerized tools don't help you in the two trickiest areas of practical state machines: assigning states and partitioning state machines so that the number of states and product terms required will actually fit within the resources of a PLD.

Other aspects of available tools allow a designer to recycle his skills from other technologies. For example, some third-party software allows an experienced TTL designer to draw a schematic comprising common TTL devices. The software then reduces the logic of a designer's schematic to a canonical sum-of-the-products form, which is—within the physical limits of PLDs—mappable over the structure of a PLD.

As an interim solution to the design problem, the recycling of existing skills is attractive. The history of engineering has numerous examples of older design methods carrying over into new technologies. But inevitably, as engineers become familiar with a new technology, they abandon their old design methods in favor of methods that exploit the characteristics of the new technology directly.

Some computerized PLD design tools embody very elaborate systems for transforming paper designs of TTL-like devices into PLD fuse patterns. For example, Altera is committed to its A+Plus software package. Indeed, the company has as many software engineers as it has device designers. Among other features, the software has a library of more than 100 TTL devices. Furthermore, the company says, the software will automatically fit and minimize a TTL design when mapping it over the structure of the company's very large and complex PLDs.

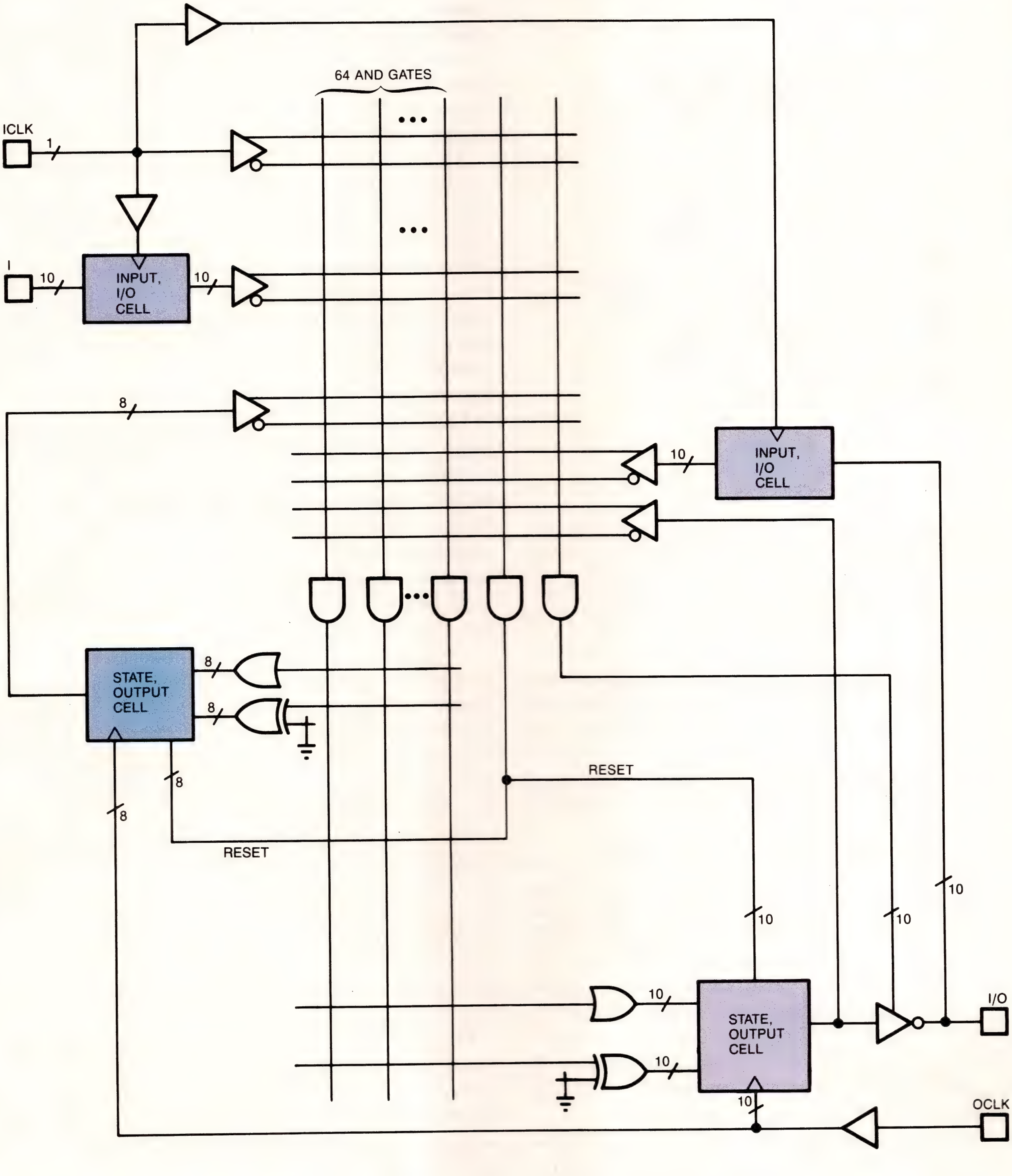


Fig 6—Combining the programmable macrocell of the 22V10 with the programmable-AND, programmable-OR structures of the FPLA, the 39V18 from Lattice Semiconductor also incorporates buried registers so that it can function as a state machine.

Some PLDs with enhanced, more flexible architectures can substitute for any of a large number of older devices.

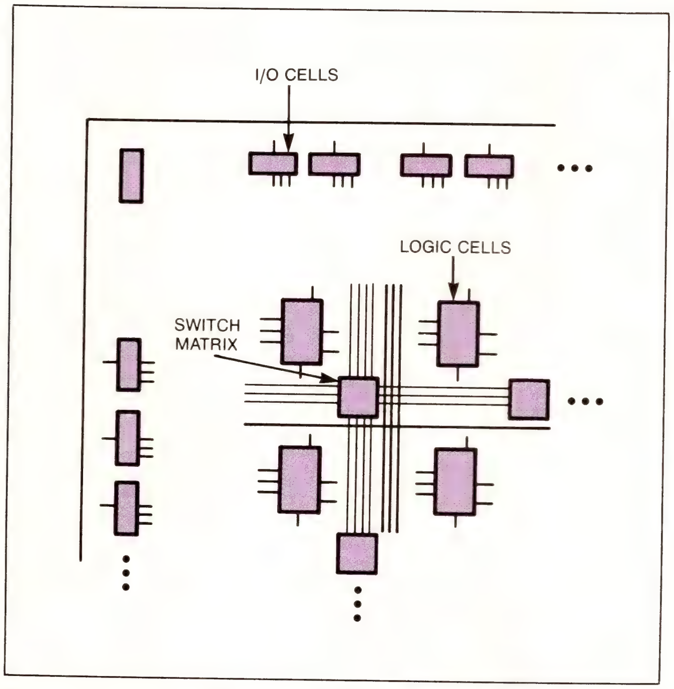


Fig 7—Sporting respective arrays of 100 and 64 programmable logic cells, *the Xilinx XC 2018 and XC 2064 have programmable I/O cells around the periphery of the chip. For interconnections, the devices have direct connections between adjacent cells; a grid of lines, with switching matrices at their intersections; and long, uninterrupted runs.*

And yet the company's own literature suggests that extracting the maximum performance from its parts requires intimate knowledge of the device itself. An application note on the TTL macros states, "These [software macros] have been designed by EPLD design experts and contain inner logic behavior to maximize EPLD speed and utilization."

The devices in the new-architecture category range from moderate extensions (more than mere enlargements) of familiar architectures to truly radical structures. The architecture of Altera's EP family of UV-erasable PLDs is an extension of the architecture of 20- and 24-pin PLDs—one that avoids the geometric expansion of fuse interconnections that would occur if the classic PLD architecture were to be simply enlarged. Altera's chip designers didn't attempt to provide for every possible interconnection between the input cells, the logic array, and the output cells.

Except for the company's 25- to 35-nsec EP300 Series devices, which are architecturally equivalent to 80% of all 20-pin PLDs, the company's larger devices are divided internally into two or four separate PLDs. An EP chip's dedicated input lines go to a global matrix that allows you to route any dedicated input to any macrocell. The macrocell differs from other PLDs' macrocells because it has a selectable logic array as well as selectable registers and I/O. Each macrocell contains three basic elements: a logic array, a flip-flop you can select for type (D, T, JK, or SR), and a selectable 3-state I/O buffer.

Altera designers did not, however, route inputs from all programmable I/O pins to the global matrix, as is the case with 20- and 24-pin PLDs. Only a fraction of the inputs from the I/O pins in a given subdivision of the chip go to the global matrix. Most of the I/O pins, in fact, feed back only to a matrix local to their subdivision. Consequently, the number of interconnections in the global matrix is far fewer than the product of the number of input pins times the number of inputs to the macrocells.

Each quadrant of an EP1800 Series device (**Fig 2** on page 115), for example, has 12 programmable I/O macrocells for a total of 48 I/O pins. The chip also has 16 dedicated input pins. Each quadrant's 12 macrocells are further divided into three groups of four: four high-speed macrocells, four macrocells that can feed back to the global matrix, and four that feed back only to the local matrix. The chip also provides a variety of clock sources for its flip-flops.

The architecture of the 78C800 Erasic from Exel (**Fig 3** on page 117) differs radically from the architecture of classic PLDs. Instead of a 2-level AND-OR structure, the 78C800 has a single plane of NOR gates. The output of each NOR gate feeds back (or, if you will, "folds back") into the input matrix of the NOR array. All of the NORs' feedback is asynchronous.

The electrically erasable, CMOS chip also has 15 buried flip-flops that are not hard-wired to output pins. The flip-flops can serve either as internal state registers or as output registers. The company states that the 78C800 is both pin compatible with existing PLDs and capable of replacing several PLDs at once, because the 78C800 deploys its internal resources more efficiently than conventional PLDs.

Because logic signals can feed back several times through the NOR matrix before emerging at an I/O pin, the company characterizes propagation delays for the current version of the 78C800 as 35 nsec from input to output with one level of logic. The delay increases by 20 nsec for each additional level.

The question designers most frequently ask the company is, how can the device work when only the NOR output, and not its complement as well, feeds back

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The added flexibility of having exactly the mix of registered and combinatorial outputs needed for a particular application is an obvious advantage for designers.

into the logic array? At first glance, the chip's designers do seem to have left out the NOR gates' complement, because other circuit elements in the chip—12 registered inputs, two dedicated inputs, 15 programmable I/O pins, and 15 flip-flops—do indeed feed both true and complement signals to the NOR array's inputs.

You can easily understand, however, why the chip's designers didn't need to include lines for the complement of the NOR gates, if you first consider that the asynchronous terms can drive only NOR gates. If you inverted the output of one of the feedback terms from a NOR gate, the inverted term would, in effect, be the OR of the gate's inputs (**Fig 4** on page 118).

Now notice that each input that feeds this resulting OR gate could instead connect directly to the following NOR gate's input. The resulting simplified circuit has exactly the same output as the circuit with the inverted NOR but has the advantage of having one logic gate fewer.

In addition to enhancing the performance of its traditional programmable logic, Signetics has also developed a unique PLD architecture. The PLHS501 random-logic unit abandons the AND-OR structure of PLDs (**Fig 5** on page 119). It consists, instead, of a single level of NAND gates. Each NAND gate's output feeds back internally to the NAND gates' input array. Feeding back one gate's output to the input of a second gate yields a NAND-NAND function that, like the classical PLD's AND-OR function, can realize any logic function.

Designers aren't limited to substituting a 2-level NAND function for an AND-OR function. Within the physical limits of the number of gates on the chip, you can configure the NAND gates into as many levels of logic as you desire, in a fashion similar to that used in Exel's 78C800.

The PLHS501 specs a propagation delay of 18 nsec for the first level of logic, plus an impressive feedback delay of only 8 nsec per additional level. The additional levels contribute such a small delay because the feedback path to the NAND array is directly from each NAND gate's output and not from the output of an output macrocell, as is the case with conventional AND-OR PLDs. The chip's output macrocells surround the central NAND core and are not connected to the NAND gates in a fixed array.

Specifically, the chip comes in a 52-pin PLCC and dissipates 250 mW typ. It has 24 dedicated inputs and eight I/O pins backed by programmable I/O macrocells. The central programmable NAND array comprises 72 NAND gates with foldback paths and 44 control NAND gates that drive the 16 dedicated outputs and eight bidirectional I/O macrocells. All 16 of the dedicated I/O pins have 3-state control lines coming from the NAND array. The dedicated output pins consist of four active-high, four active-low, and eight X-OR outputs. NAND gates from the central array control pairs of outputs. Internal logic enables four of the eight bidirectional pins, while fuses control the remaining four.

Lattice Semiconductor is also making a cautious foray into the realm of large extensions to the basic PLD architecture with its 39V18 (**Fig 6** on page 121). First, the electrically erasable device has an FPLA core of a programmable-AND array and a programmable-OR array. Second, this jam-packed 24-pin device has both programmable I/O macrocells and input macrocells, as well as buried registers so that it can function as a state machine. The 10 I/O macrocells have two 64-input sum terms with programmable polarity, and they can function as combinatorial or registered outputs. In the registered mode, you can use a common clock for all the output flip-flops or clock each individual flip-flop with one of the 64-input sum terms. Third, in addition to the 10 I/O macrocells, the device has eight similar cells that compose a buried state register.

The 39V18's programmable input macrocells mark a departure from conventional PLDs, and indeed, a departure from most of the recent enhancements to PLD architecture. The 10 input macrocells have the same input structure as the input section of the I/O macrocells, and they can function either as transparent, clocked latches or as registers.

The Xilinx XC 2018 and XC 2064 are, by any reasonable definition of the term, PLDs, but their architecture (**Fig 7** on page 122) sets them far apart from any of the other devices described here. The two chips are programmble gate arrays. The XC 2018, which is the equivalent of 1800 two-input NAND gates, comprises three user-programmable elements: I/O blocks, configurable logic blocks, and interconnections.

Internally, both chips have a square array of configurable logic macrocells surrounded by a hollow rectangle of programmable I/O macrocells. The XC 2064 has 64 configurable logic macrocells; the XC 2018 has 100.

You can program the I/O macrocells for TTL or CMOS levels. The I/O macrocells also have a selectable flip-flop in the input path. The configurable logic macrocells have four inputs and a clock line. The macrocells

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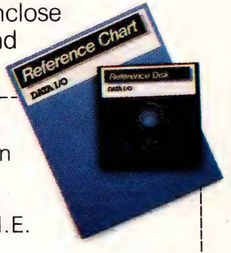

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CIRCLE NO 72

use a look-up-table scheme to provide any Boolean function of the four inputs (or any two functions of three variables). Like other logic macrocells, the Xilinx cells have a D flip-flop that serves as a storage element, plus multiplexers to enable various combinatorial and registered outputs from the cell.

The chips offer you three ways to interconnect the various cells: direct connections between adjacent cells; a grid of lines, with switching matrices at their intersections, that surround the blocks with a rectangular grid; and long, uninterrupted runs for global signals that cannot tolerate the delays incurred in the switching matrices.

Static RAMs provide logic links

A unique feature is that the devices don't use any of the schemes employed in other PLDs for configuring. The devices have no fuses and no UV-erasable or electrically erasable links. Instead, they employ static-CMOS RAM cells to enable interconnections and define logic functions.

You load this internal RAM during initialization upon powering up a system. The device can load itself from an external PROM, or you can initialize the chip just as you would any other μP peripheral chip from system ROM or from disk.

In addition to PLDs making further inroads into ASIC territory, you can expect manufacturers soon to begin combining classical PLDs with other functional elements on the same chip. Harris's HPL-82C339 programmable chip-select decoder is an example of a PLD enhanced with additional circuitry dedicated to a special purpose.

Another part, AMD's Am29PL141 fuse-programmable controller, comprises a sequencer, a 64-word×32-bit PROM, and a 32-bit output register on a single chip. MMI's Prose combines a PLD and a PROM. The Prose's PROM works in the same way the control-store PROM of a bit-slice machine does, while the PLD takes the place of the bit-slice's controller.

Intel will soon introduce the 5CBIC, which is a programmable bus-interface controller. The IC will transfer data to and from a computer's bus, and it will take care of control-logic signals. Other new entries to the PLD realm that you can expect to see are register-intensive functions like counters and shifters. **EDN**

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

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The *NEW* TI-95 Procalc™

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Scientific Calculator

- Introduces "windows" to programmable-calculators! Display windows identify the operations performed by the TI-95's redefinable function keys.
- Packs an unprecedented 200-plus functions in a menu-oriented, easy-to-use package.
- 8K RAM expandable to 16K
- Up to 900 data registers. Or up to 7200 program steps. Or up to 6200 bytes of file space for storing custom programs or data.
- An unprecedented set of built-in scientific functions including permutations, combinations, least common multiple, prime factors, random number generation, metric conversions, hyperbolic trigs and cubic- and quadratic-equation evaluation.
- Straightforward keystroke language includes branching, subroutines, tests, flags, file operations and alpha capability.
- Full program control of redefinable function keys
- AOS™ algebraic operating system
- The TI-95 comes with a comprehensive user's guide, a programming guide, a sturdy hard-plastic carry case, and 4 AAA size batteries.
- Constant memory feature 3.75″ x 8″ x 1″

Mfr. Sugg. Ret. $200 **$139**

TI-74 Basicalc™

- It's an advanced scientific calculator, with 70 functions—and a BASIC programmable calculator, with 113 commands.
- AOS™ algebraic operating system
- 8K bytes of built-in RAM, plus optional 8K
- Display shows up to 31 large alphanumeric characters (scrolls left or right to 80) and 14 status indicators. Adjustable contrast.
- Comes with user's guide and a BASIC programming reference guide.
- Scientific functions include common and natural logarithms and antilogarithms, reciprocals, powers, roots, factorials, and trigonometric calculations, including inverses, in degrees, radians or grads.
- Constant memory feature 4.2″ x 8.3″ x 1.3″

Mfr. Sugg. Ret. $135 **$94**

TI-74 and TI-95 Accessories		Mfr. Sugg. Ret.	Elek-Tek Price
TI-8K	Constant Memory Cartridge	$ 50.00	$34.00
TI-PC 324	Printer	115.00	69.00
TI-CI-7	Cassette Interface	35.00	22.00
Software Cartridges			
TI-74	Learn Pascal Cartridge	$45.00	$29.00
TI-74	Statistics Cartridge	45.00	29.00
TI-74	Mathematics Cartridge	45.00	29.00
TI-95	Mathematics Cartridge	50.00	33.00
TI-95	Statistics Cartridge	50.00	33.00

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CIRCLE NO 23

TABLE 1—PROGRAMMABLE LOGIC DEVICES

MANUFACTURER	DEVICES	TECHNOLOGY	DESCRIPTION
ADVANCED MICRO DEVICES INC BOX 3453, SUNNYVALE, CA 94088 PHONE (408) 732-2400	20-PIN PALs	TTL	HIGH-SPEED, ½- AND ¼-POWER VERSIONS
	AmPAL18P8	TTL	SUPERSET OF COMBINATORIAL 20-PIN PALs
	AmPAL22V10	TTL	24-PIN PAL, OUTPUT MACROCELLS, 8 OR 16 TERMS/OUTPUT
	AmPAL23S8	TTL	20-PIN PAL-BASED SEQUENCER, 6 BURIED REGISTERS
	AmPAL20EV8/ 20EG8	TTL/ECL	125-MHz, 22V10-LIKE, 10KH AND 100K ECL VERSIONS
	24-PIN PALs	TTL	HIGH-SPEED, REGISTERED, AND COMBINATORIAL
	ENHANCED 24-PIN PALs	TTL	SUPERSET OF 24-PIN PALs, PROG POLARITY, ADDITIONAL PRODUCT TERMS AND I/O
	XOR 24-PIN PALs	TTL	PROGRAMMABLE POLARITY, ADDITIONAL TERMS
	29PL141	TTL	FUSE-PROGRAMMABLE CONTROLLER
ALTERA CORP 3525 MONROE ST, SANTA CLARA, CA 95051 PHONE (408) 984-2800	EP310, 320	EPROM CMOS	SUPERSET OF 20-PIN PALs, ZERO STANDBY POWER
	EP600, 900	EPROM CMOS	24- AND 40-PIN, MULTIPLE-PLD EQUIVALENT
	EP1210, 1800	EPROM CMOS	1200-, 2000-GATE EQUIVALENT PLDs
AMTEL CORP 2095 RINGWOOD AVE, SAN JOSE, CA 95131 PHONE (408) 434-9201	AT 22V10	EPROM CMOS	24-PIN PAL, 132 TERMS, 10 SUM, 10 FLIP-FLOPS, 22 ARRAY INPUTS
	AT V750	EPROM CMOS	24-PIN PAL, 171 TERMS, 20 SUM, 20 FLIP-FLOPS, 42 ARRAY INPUTS
CYPRESS SEMICONDUCTOR CORP 3901 N FIRST ST, SAN JOSE, CA 95134 PHONE (408) 943-2666	PAL C 20 SERIES	EPROM CMOS	STANDARD AND HIGH-PERFORMANCE VERSIONS AT 45 mA
	PLD C 20G10	EPROM CMOS	EMULATES 10 24-PIN PALs, STD AND HIGH PERFORMANCE AT 55 mA
	PAL C 22V10	EPROM CMOS	COMMERCIAL, MILITARY VERSIONS, ½-POWER
EXEL MICROELECTRONICS 2150 COMMERCE DR, SAN JOSE, CA 95131 PHONE (408) 942-0500	ERASIC 78C800	EE CMOS	FOLDED NOR LOGIC WITH ASYNCHRONOUS FEEDBACK
FAIRCHILD SEMICONDUCTOR CORP BOX 5000, PUYALLUP, WA 98373 PHONE (800) 554-4443	FASTPLA	TTL	16PX, 16RX, 16LX 20-PIN PALs, POWER-UP RESET
	932459	TTL	28-PIN FPLA
GOULD ELECTRONICS INC 3800 HOMESTEAD RD, SANTA CLARA, CA 95051 PHONE (408) 246-0330	18CV8	EE CMOS	SUPERSET OF 20-PIN PALs, PROGRAMMABLE MACROCELLS
	22CV10	EE CMOS	22V10 COMPATIBLE
	22CP10	EE CMOS	PLS 173 COMPATIBLE, 20-PIN FPLA
	18CP210	EE CMOS	PLS 153 COMPATIBLE, 24-PIN FPLA
HARRIS CORP BOX 1239, MELBOURNE, FL 32901 PHONE (305) 724-3576	HPL-82CX38, HPL-82X39	FUSE CMOS	PROGRAMMABLE CHIP-SELECT DECODERS LIKE 74138/139
	HPL-16XXX	FUSE CMOS	20-PIN-PAL COMPATIBLE
	HPL-82C339	FUSE CMOS	PROGRAMMABLE CHIP-SELECT DECODER
INTEL CORP 151 BLUE RAVINE RD, FOLSOM, CA 95630 PHONE (916) 351-8080	5C060	EPROM CMOS	ALTERA EP600 SECOND SOURCE
	5C121	EPROM CMOS	ALTERA EP1200 SECOND SOURCE
	5CBIC	EPROM	PROGRAMMABLE BUS-INTERFACE CONTROLLER

*UNLESS OTHERWISE SPECIFIED.
**EP600 ONLY
†SOFTWARE TOOLS:
A = PROPRIETARY
B = MMI'S PALASM
C = SIGNETICS'S AMAZE

PERFORMANCE: MAX PROP DELAY, INPUT TO OUTPUT (nSEC)*	MAX POWER-SUPPLY CURRENT (mA)*	COST: PLASTIC DIPs (100 QUANTITY)*	SOFTWARE TOOLS†	READER SERVICE NUMBER
15, 25, 35	180, 155, 90, 80, 45	FROM $3.10	D E F G	CIRCLE NO 650
15, 25, 35	180, 90, 55	FROM $3.10	D E F G	
25, 35	180	FROM $10.70	D E F G	
20, 25	200	FROM $15.65	D E G	
6	230	FROM $22.80	D E G	
15, 20, 25	210, 165, 105	FROM $5.85	D E F G	
15, 25	210, 105	FROM $8.25	D E F G	
20, 30, 40	210, 180, 90	FROM $6.95	D E F G	
20-MHz CLOCK	400, 450	FROM $32.50 (CERAMIC)	A	
25, 35, 45	1 mA/MHz (10 μA DC)	$4.50	A D E F G	CIRCLE NO 651
25, 45, 55	2 mA/MHz (10 μA DC)	$10.75, $17.50	A D E** F G	
15, 20, 25 MHz	3 mA/MHz (10 μA DC)	$44	A F	
25	5	$7.50 (1000)	D E	CIRCLE NO 652
30	100	$7.50 (1000)		
20, 25, 35	45	FROM $3.55 (PLASTIC), $13.50 (WINDOW)	D E F G	CIRCLE NO 653
25, 35	55	FROM $6.75 (PLASTIC), $14.65 (WINDOW)	D E	
25, 35	90	FROM $11.95 (PLASTIC), $36 (WINDOW)	D E F G	
35 PLUS 20/LOGIC LEVEL	35 (QUIESCENT)	BETWEEN $20 AND $30 (SAMPLES), BETWEEN $10 AND $12 (PRODUCTION)	A + D	CIRCLE NO 654
15, 25	170	LXB $4, LXA $1.85, PXB $5.38, PXA $2.10	D E F G	CIRCLE NO 655
15	180	$5.49	D E	
25, 35, 50	25 + 1 mA/MHz	$4.42	D	CIRCLE NO 656
25, 35, 50	45 + 1 mA/MHz	$6.15	D F	
30	35 + 1 mA/MHz	$5.23	D F	
30	35 + 1 mA/MHz	$5.23	D F	
50	1/MHz	FROM $6.44 (COMMERCIAL), $17.94 (HI-REL)	D F	CIRCLE NO 657
125	6/MHz	FROM $9.68 (COMMERCIAL), $34.55 (HI-REL)	D E F G	
25	2 (TYP)	—	A	
35	—	—	A D E G	CIRCLE NO 658
50	—	$55 (1000)	A	
BMU 25, 35, 45 PLU 65, 75, 85	375 μW	$17 (100)	A	

D = DATA I/O-FUTURENET'S DASH-ABEL (BOX 97046, REDMOND, WA 98073. PHONE (206) 881-6444. CIRCLE NO 668)
D* = DATA I/O-FUTURENET'S DASH-GATES
E = P-CAD'S CUPL (1290 PARKMOOR AVE, SAN JOSE, CA 95126. PHONE (408) 971-1300. CIRCLE NO 669)
F = VALLEY DATA SCIENCES' PERFECT (2426 CHARLESTON RD, MOUNTAIN VIEW, CA 94043. PHONE (415) 968-2900. CIRCLE NO 670)
G = KONTRON'S LOG/ic (633 CLYDE CT, MOUNTAIN VIEW, CA 94039. PHONE (415) 965-7020. CIRCLE NO 671)
G* = KONTRON + AMAZE

Table continued on pg 130

TABLE 1—PROGRAMMABLE LOGIC DEVICES *(Continued)*

MANUFACTURER	DEVICES	TECHNOLOGY	DESCRIPTION
LATTICE SEMICONDUCTOR CORP 15400 NW GREENBRIER PKWY, BEAVERTON, OR 97006 PHONE (503) 629-2131	GAL 16V8	EE CMOS	SUPERSET OF 20-PIN PALs, ½-, ¼-POWER VERSIONS
	GAL 20V8	EE CMOS	SUPERSET OF 24-PIN PALs, ½-, ¼-POWER VERSIONS
	ispGAL1628	EE CMOS	IN-CIRCUIT PROGRAMMABLE SUPERSET 20-PIN PALs
	GAL39V18	EE CMOS	FPLA WITH 8 BURIED REGISTERS, SUPERSET OF 22V10, 32V10, 825XXX, EP6XXX
MONOLITHIC MEMORIES INC 2175 MISSION COLLEGE BLVD, SANTA CLARA, CA 95054 PHONE (408) 970-9700	20-PIN PAL/HAL	TTL, EPROM CMOS	VERY HIGH-SPEED, ½-, ¼-POWER VERSIONS
	24-PIN PAL/HAL	TTL	HIGH-SPEED, ½-POWER VERSIONS
	PAL20RA10, 16RA8	TTL	REGISTERED ASYNCHRONOUS 20/24-PIN PALs
	PAL6L16A, 8L14A	TTL	DECODING PLDs WITH ONE AND ARRAY
	MEGAPAL	TTL	REGISTERED PAL, 64 INPUTS, 32 OUTPUTS
	ZHAL 20/24/84	MASKED CMOS	20/24/84-PIN, ZERO STANDBY POWER
	PAL32VX10	TTL	24-PIN, PROGRAMMABLE MACROCELLS
	PAL22RX8	TTL	24-PIN, PROGRAMMABLE FLIP-FLOPS
	PMS14R21	TTL	24-PIN, HIGH-SPEED SEQUENCER, 128 STATES
	PAL22CV10	TTL	24-PIN, VARIABLE PRODUCT TERMS, MACROCELLS
	ZPAL24 SERIES	EPROM CMOS	24-PIN, ZERO STANDBY PAL
	PAL22V10B	EPROM CMOS	24-PIN, VARIABLE PRODUCT TERMS, MACROCELLS
	M2064 LCA	CMOS	SECOND SOURCE XILINX XC2064
NATIONAL SEMICONDUCTOR CORP BOX 58090, SANTA CLARA, CA 95052 PHONE (408) 721-5000	20-PIN PALs	TTL	HIGH-SPEED, ½-, ¼-POWER VERSIONS
	24-PIN PALs	TTL	ULTRAFAST, FAST, AND STANDARD VERSIONS
	PALC16F8	FUSED CMOS	PROGRAMMABLE-OUTPUT, PAL-COMPATIBLE
	ECL PALs	TTL	24-PIN ECL PALs
	PL21F10	TTL	ASYNCHRONOUS, REGISTERED FPLA, PROG I/O
PANATECH SEMICONDUCTOR 3375 SCOTT BLVD, #440, SANTA CLARA, CA 95054 PHONE (408) 727-7700	20-PIN PALs	EPROM CMOS	PAL-COMPATIBLE, PROGRAMMABLE POLARITY, OTP
	22V10A	EPROM CMOS	24-PIN PAL, I/O MACROCELLS
SIGNETICS CORP BOX 3409, SUNNYVALE, CA 94088 PHONE (408) 991-2000	PROG GATE ARRAYS	TTL	20-, 28-PIN AND ARRAY WITH FEEDBACK
	ADDRESS DECODERS	TTL	AND ARRAY, 24-PIN VERSION
	FPLA	TTL-CMOS	20-, 24-, 28-PIN, PROG-AND, PROG-OR ARRAYS
	FPLA	TTL	20-PIN, FIXED-OR ARRAY
	FPLS	TTL	20-, 24-, 28-PIN SEQUENCERS, FPLA, BURIED REGISTERS
	PML	TTL, CMOS	52-PIN PLCC, SINGLE NAND ARRAY WITH FEEDBACK
SPRAGUE SOLID STATE 3900 WELSH RD, WILLOW GROVE, PA 19090 PHONE (215) 657-8400	20-PIN PALs	EPROM CMOS	COMPATIBLE WITH 16LC8, 18RC8, 16RC6, 16RC4 PALs

*UNLESS OTHERWISE SPECIFIED.
**EP600 ONLY
†SOFTWARE TOOLS:
A = PROPRIETARY
B = MMI'S PALASM
C = SIGNETICS'S AMAZE

PERFORMANCE: MAX PROP DELAY, INPUT TO OUTPUT (nSEC)*	MAX POWER-SUPPLY CURRENT (mA)*	COST: PLASTIC DIPs (100 QUANTITY)*	SOFTWARE TOOLS†	READER SERVICE NUMBER
15, 25, 35 COMMERCIAL,	90, 45	$3.57-$6.92 (COM), $11.59-$25.61 (MIL)	D E F G	CIRCLE NO 659
20, 30 MILITARY	90, 45		D E F G	
25, 35 (COM), 30 (MIL)	90	$25 (SAMPLES)	D E F	
15, 30 (COM), 35 (MIL)	120	$20 (SAMPLES)	D	
10, 15, 25, 35	180, 90, 55, 40	FROM $3.34	B D E F G	CIRCLE NO 660
15, 25, 30, 35	210, 105, 55	FROM $5.29	B D E F G	
20, 30	200, 170	FROM $8.56	B D E F G	
25	90	FROM $5.29	B D E G	
40, 50	640, 280	FROM $33.40	B D E F G	
25	0 (DC)	FROM $1.95 + MASK CHARGE	B D E G	
25, 30	180	FROM $13.28	B D F G	
25	210	FROM $6.50	B D G	
25 MHz	200	FROM $29.95	B D G	
25, 35	80	FROM $9.95	B D E	
35, 45	0 (DC)	FROM $7.95	B D E	
15	180	FROM $29.95	B D E G	
20, 33, 50 MHz	40-80	$26, $32, $46 (1000)	B	
15, 25, 30, 35	180, 90, 45	FROM $3.05 (COM), $5.20 (MIL)	D E F G	CIRCLE NO 661
15, 25, 50	210, 180	FROM $5.45 (COM), $12.75 (MIL)	D* E F G	
35	6/MHz	$16	D	
6	220	FROM $19.85	D E	
20, 25	200, 180	$27.50	D	
35, 55	60, 10	$2.25 TO $3.25 (1000)	A D E F G	CIRCLE NO 662
25	120 MAX, 80 TYP	$8 (1000)	A D E F	
25, 35	170, 155	$2.80 (DIP), $3.29 (PLCC)	C D E F G*	CIRCLE NO 663
30	155	$2.40 (DIP), $2.82 (PLCC)	C D E F G*	
30, 40, 50	170, 155	$2.90 (DIP), $3.41 (PLCC)	C D E F G*	
20	155	$2.10 (DIP), $2.47 (PLCC)	C D E F G*	
25, 45, 55, 60 TYP	225, 190, 180	$3.50 TO $13, $4.12 TO $15.30	C D E F G*	
18 + 8 nSEC/LEVEL	325	FROM $26.99 (PLCC)	C D G*	
45, 55, 70	65	$3.20 (PLASTIC), $7.95 (WINDOW)	D E F G	CIRCLE NO 664

D = DATA I/O-FUTURENET'S DASH-ABEL (BOX 97046, REDMOND, WA 98073. PHONE (206) 881-6444. CIRCLE NO 668)
D* = DATA I/O-FUTURENET'S DASH-GATES
E = P-CAD'S CUPL (1290 PARKMOOR AVE, SAN JOSE, CA 95126. PHONE (408) 971-1300. CIRCLE NO 669)
F = VALLEY DATA SCIENCES' PERFECT (2426 CHARLESTON RD, MOUNTAIN VIEW, CA 94043. PHONE (415) 968-2900. CIRCLE NO 670)
G = KONTRON'S LOG/ic (633 CLYDE CT, MOUNTAIN VIEW, CA 94039. PHONE (415) 965-7020. CIRCLE NO 671)
G* = KONTRON + AMAZE

Table continued on pg 132

TABLE 1—PROGRAMMABLE LOGIC DEVICES *(Continued)*

MANUFACTURER	DEVICES	TECHNOLOGY	DESCRIPTION
TEXAS INSTRUMENTS INC BOX 225012, DALLAS, TX 75265 PHONE (800) 232-3200	20-PIN PALs	TTL	HIGH-SPEED, ½-POWER VERSIONS
	24-PIN PALs	TTL	HIGH-SPEED REGISTERED VERSIONS
	FPLAs	TTL	3-STATE (-839) OR OPEN-COLLECTOR (-840) OUTPUTS
	FPLSs	TTL, EPROM CMOS	FPLA WITH BURIED REGISTERS
	20X SERIES	TTL	EXOR PALs
	TIBPALR19XX	TTL	REGISTERED-INPUT PALs
	TIBPALT19XX	TTL	LATCHED-INPUT PALs
VLSI TECHNOLOGY INC 1109 MCKAY DR, SAN JOSE, CA 95131 PHONE (408) 434-3100	VP16RP8M, 20RP8M	MASKED CMOS	HARD-WIRED REPLACEMENT FOR 20- AND 24-PIN PALs
	VP16V8E, VP20V8E	EE CMOS	SUPERSET OF 20- AND 24-PIN PALs
XILINX INC 2069 HAMILTON AVE, SAN JOSE, CA 95125 PHONE (408) 559-7778	XC-2064 LCA	CMOS (RAM FUSES)	1200-GATE PROGRAMMABLE GATE ARRAY
	XC-2018 LCA	CMOS (RAM FUSES)	1800-GATE PROGRAMMABLE GATE ARRAY

*UNLESS OTHERWISE SPECIFIED.
**EP600 ONLY
†SOFTWARE TOOLS:
A = PROPRIETARY
B = MMI'S PALASM
C = SIGNETICS'S AMAZE
D = DATA I/O-FUTURENET'S DASH-ABEL (BOX 97046, REDMOND, WA 98073. PHONE (206) 881-6444. CIRCLE NO 668)
D* = DATA I/O-FUTURENET'S DASH-GATES
E = P-CAD'S CUPL (1290 PARKMOOR AVE, SAN JOSE, CA 95126. PHONE (408) 971-1300. CIRCLE NO 669)
F = VALLEY DATA SCIENCES' PERFECT (2426 CHARLESTON RD, MOUNTAIN VIEW, CA 94043. PHONE (415) 968-2900. CIRCLE NO 670)
G = KONTRON'S LOG/ic (633 CLYDE CT, MOUNTAIN VIEW, CA 94039. PHONE (415) 965-7020. CIRCLE NO 671)
G* = KONTRON + AMAZE

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You also have access to applications support that's second to none. With complete, up-to-date hardware/software documentation.

ZIATECH CONTROL: FROM

PERFORMANCE: MAX PROP DELAY, INPUT TO OUTPUT (nSEC)*	MAX POWER-SUPPLY CURRENT (mA)*	COST: PLASTIC DIPs (100 QUANTITY)*	SOFTWARE TOOLS†	READER SERVICE NUMBER
12, 15, 25, 35	200, 180, 100, 90	FROM $3.61 (1000)	D E F G	CIRCLE NO 665
20, 25	210, 180	FROM $6.15 (1000)	D E F G	
20	180	$6.14 (1000)	D E F	
50 MHz	180	$26.71 (1000)	D E	
20	180, 165	$7.94 (1000)	D E F G	
25	210	$7.94 (1000)	D E G	
25	210	$7.94 (1000)	D E G	
25, 35	2 mA/MHz	$2.15 (5000)	D E F G	CIRCLE NO 666
25, 35	90	$3.20 (5000)	D E F G	
70 MHz	40-80	FROM $23	A D*	CIRCLE NO 667
70 MHz	50-90	FROM $48	A D*	

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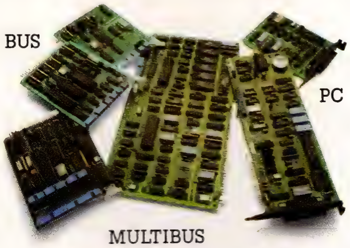

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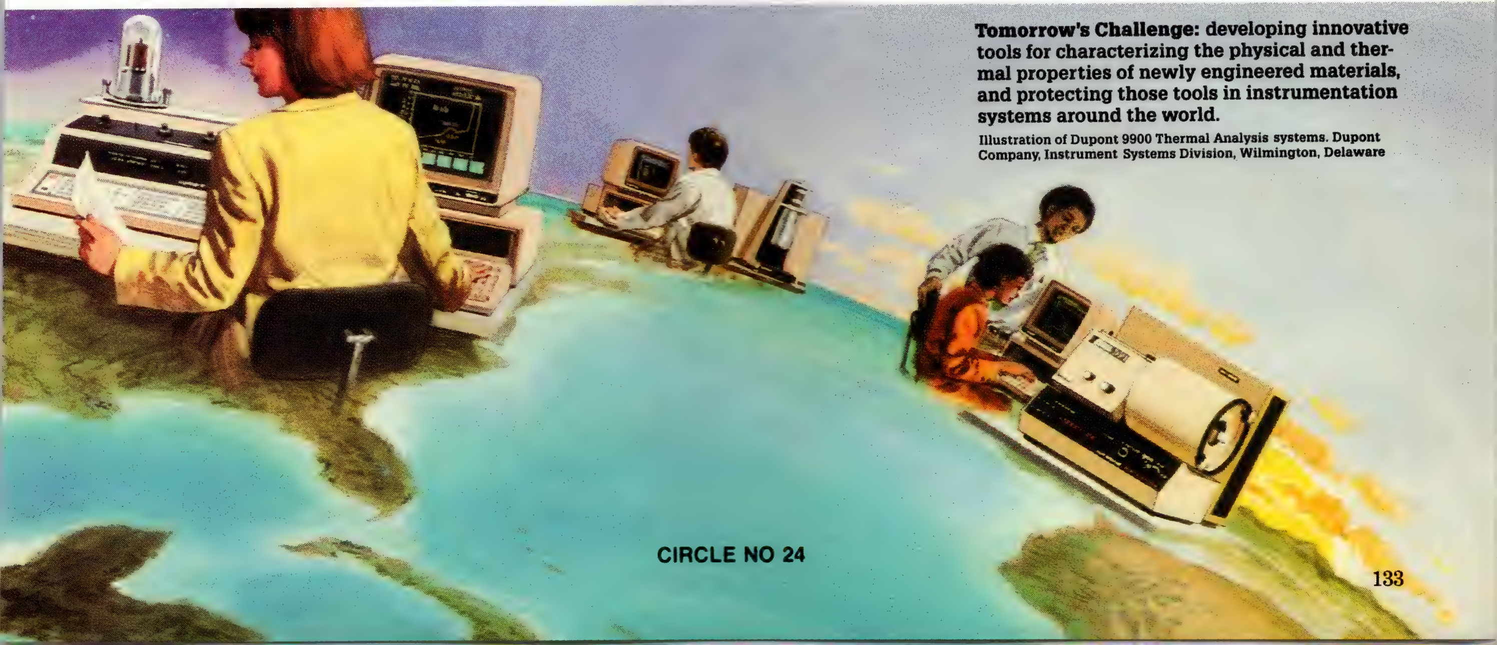

Tomorrow's Challenge: developing innovative tools for characterizing the physical and thermal properties of newly engineered materials, and protecting those tools in instrumentation systems around the world.

Illustration of Dupont 9900 Thermal Analysis systems. Dupont Company, Instrument Systems Division, Wilmington, Delaware

CIRCLE NO 24

THE PROGRAMMABLE GATE YOU'VE ALWAYS WANTED.

We don't mean to be wishy-washy, it's just that our Programmable Gate Array delivers both more of what you want and less of what you don't.

Unlike a conventional gate array which is cast in cement at the factory, the Programmable Gate Array is user-programmable. So there's no risk in design or inventory. And that makes it a lot less dicey.

As in, more speed and less money.

More density and less risk.

And more design flexibility but less time to market.

How can one part offer so much?

By combining the advantages of VLSI with the advantages of programmability. And eliminating the disadvantages.

"OF COURSE. A PROGRAMMABLE GATE ARRAY."

That's what logic designers said when we asked them if they could describe the ideal logic device.

We couldn't agree more. Just look at the benefits of such a device.

You get the wide open architecture of a gate array, without the penalties. The NRE, the long development time, the inventory risk, the limited testability, and last but certainly not least, the 50-50 chance that system changes may mean another pass.

Instead, you get programmability. Unlimited reprogrammability. No NRE. A development cycle you can measure on one page of a month-to-month calendar. And a standard part that arrives on your doorstep already tested 100% perfect down to the last transistor.

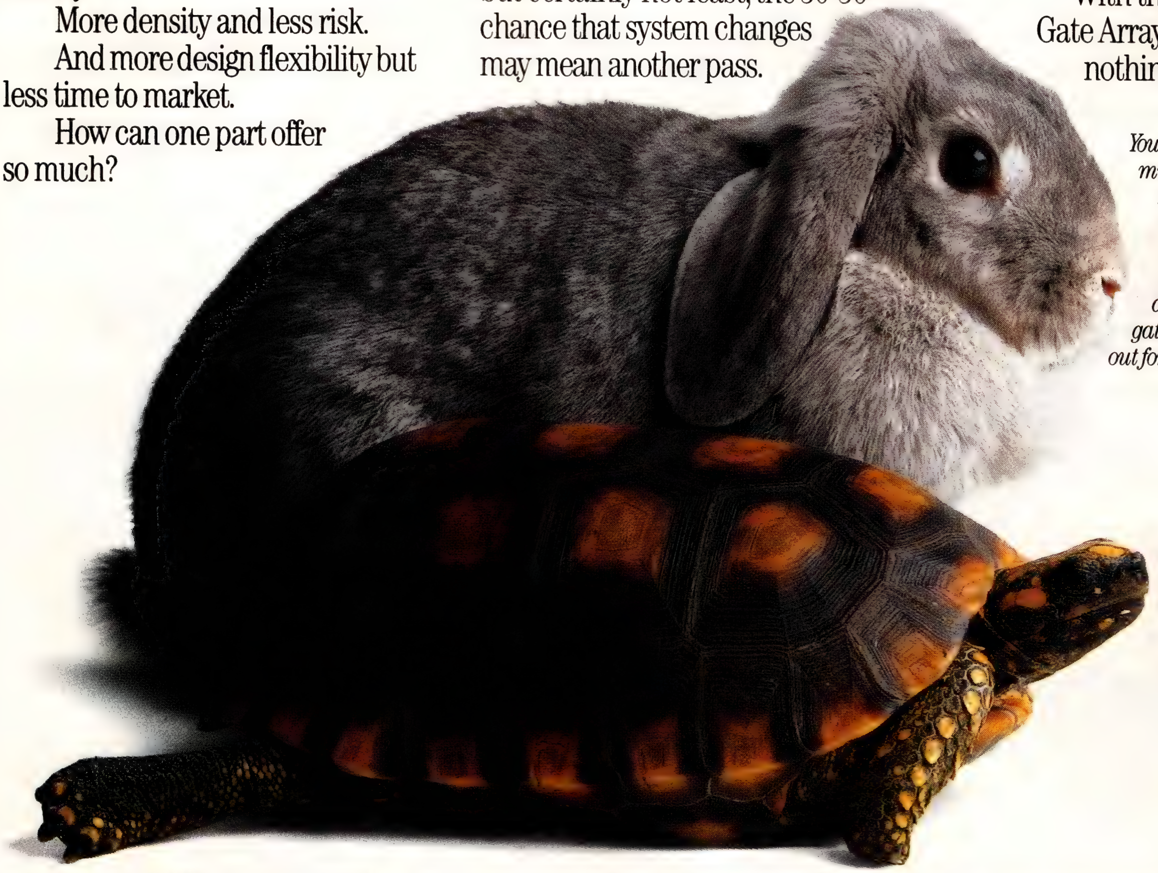
You can't beat it with a stick.

SPEED, DENSITY, PRICE. PICK ANY THREE.

Until the Programmable Gate Array, logic design was a frustrating game of give and take.

You gave up certain things as limited logic solutions took away your options.

With the Programmable Gate Array, you give up nothing.



You might not expect much speed in a part like this. But at 70 MHz, the Programmable Gate Array is more than fast enough for most applications. And with 1800 gates to work with, why shell out for a bunch of little PLDs?

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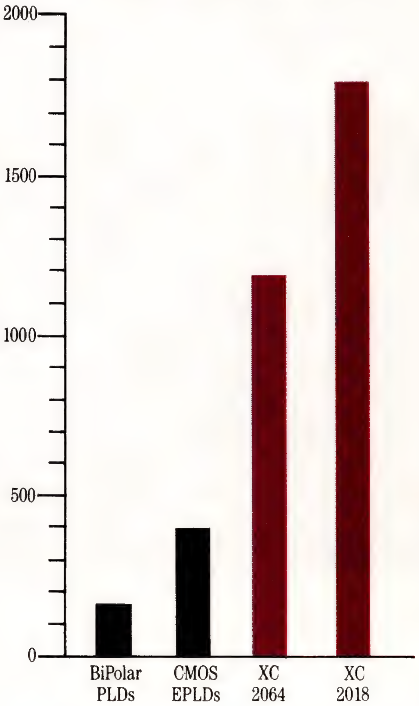

Other PLDs claim lots of gates, but their restrictive architectures only let you use a small fraction of them. Our patented Logic Cell Array architecture is more open. So you can use all the gates we claim. And there are more chips—with more gates—on the way.

After all, why use anything else when the Programmable Gate Array gives you so much more? And, so much less.

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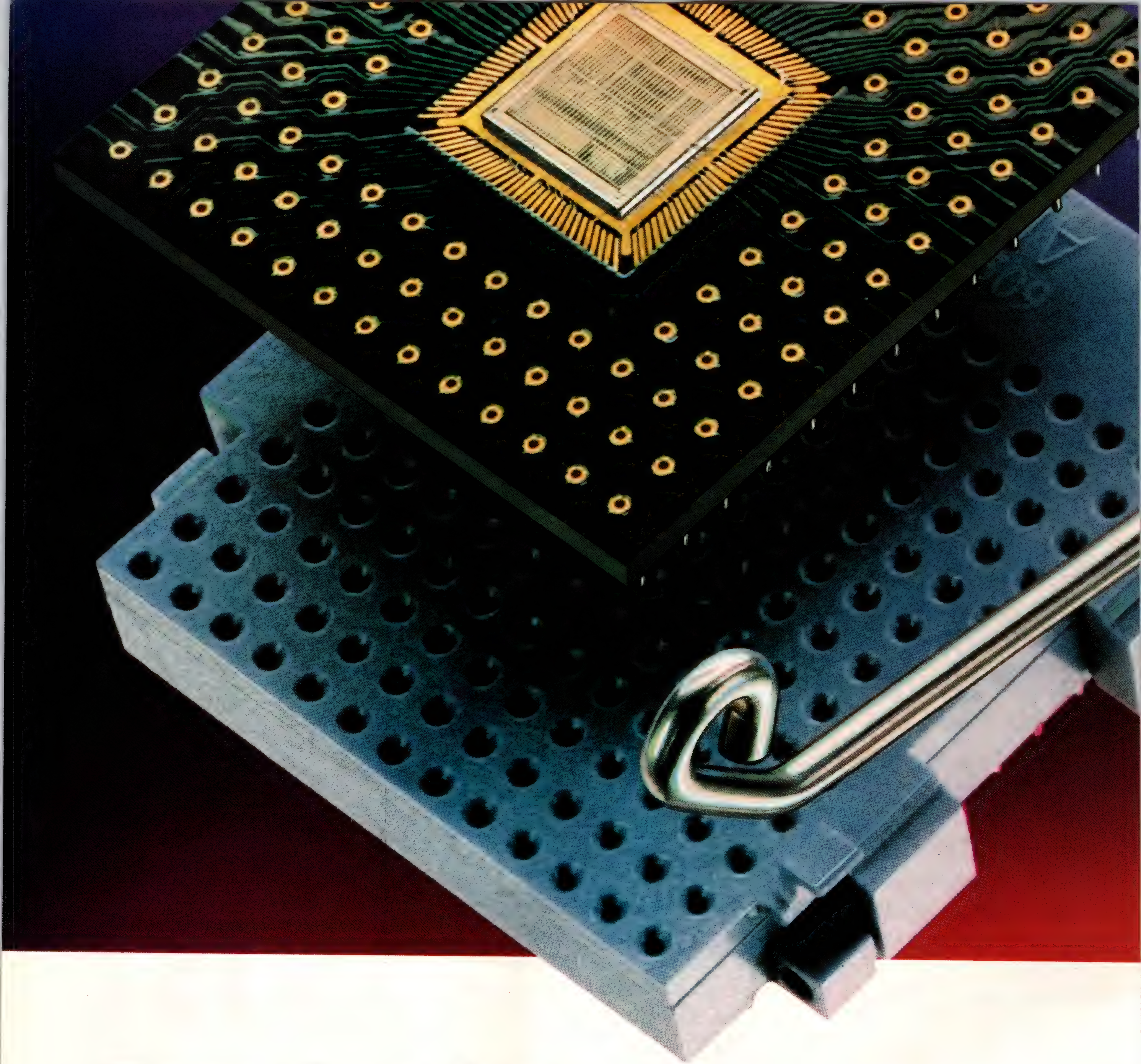
CIRCLE NO 73



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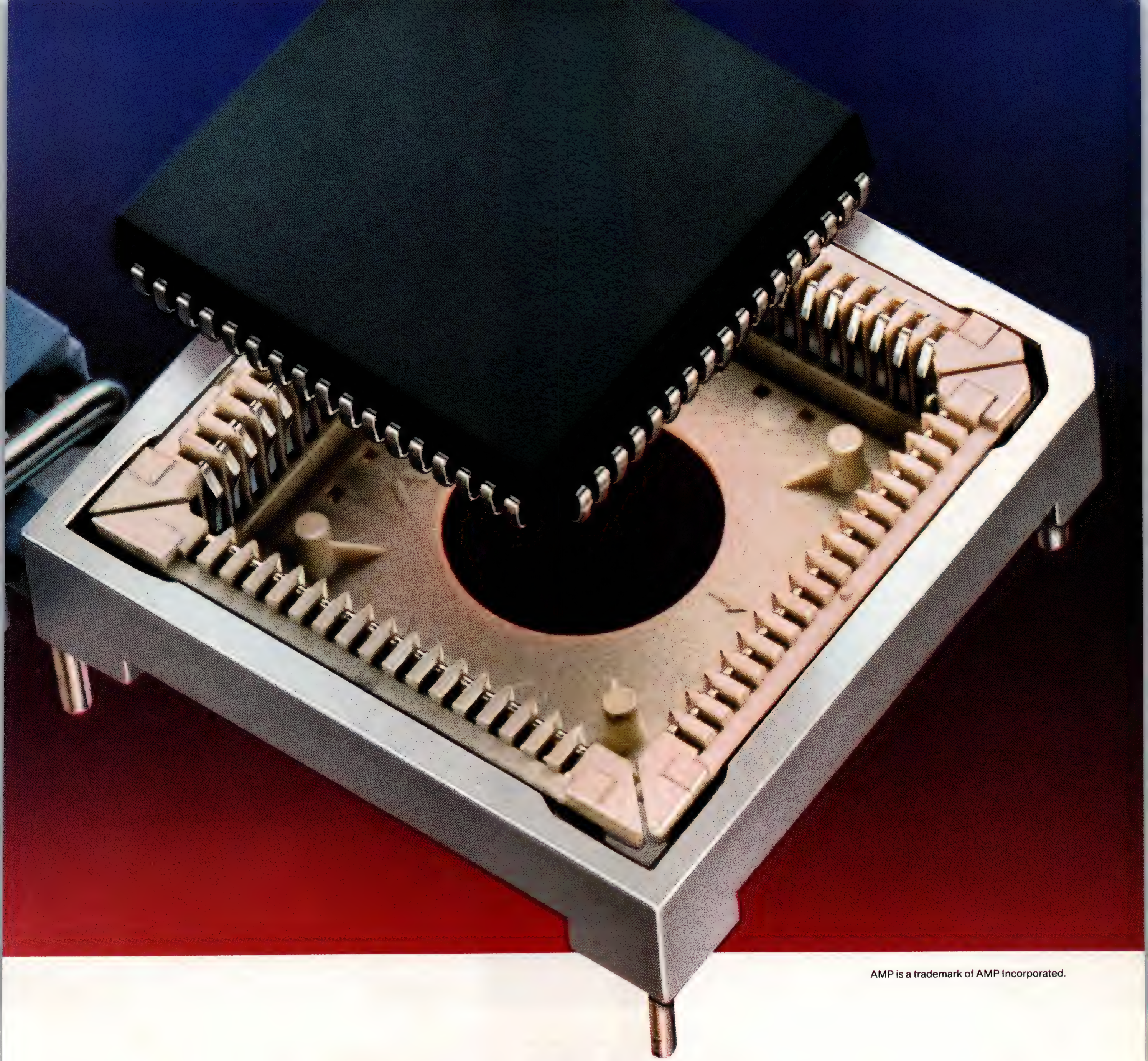

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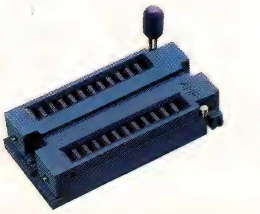
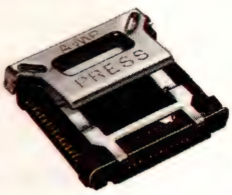
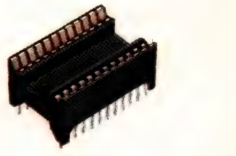


Press-to-release hinged cover on low height burn-in socket eliminates tools, eliminates loose parts. Low profile gets more on the board.



Low-cost DIP sockets for burn-in and test applications feature fast and simple below-package sword slot unloading.



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CIRCLE NO 74

Hardware methods improve 1-chip A/D converters

By using progressive clocking, a sliding-scale technique, and error-correction methods, you can improve the speed and the differential linearity of 1-chip successive-approximation A/D converters. Thus, in a given application, you can use a lower-cost A/D converter than would otherwise be possible.

Steven Sidman and Steven Harris
Advanced Micro Devices Inc

Many scientific applications for A/D converters impose stringent requirements on such parameters as conversion speed, dynamic range, and differential linearity; these rigorous requirements sometimes preclude the use of cost-effective monolithic integrated circuits. You can, however, use progressive clocking, the Gatti sliding-scale technique, and error-correction methods with low-cost, monolithic 12-bit successive-approximation ADCs to reduce conversion time by 20 to 40% and to improve the ADCs' differential linearity.

In the following sections, you'll find data showing differential linearity and effective resolution as a function of the clocking method (fixed-rate, 2-speed, and multispeed), as well as a short description of the automated test setup used to measure these parameters under dynamic conditions. In addition, the text describes the Gatti sliding-scale technique **(Ref 1)** and error-correction schemes that you can easily apply to one or more integrated A/D converters. First, though, it's important that you understand an ADC's crucial differential-nonlinearity parameter.

DNL determines bit width

Differential nonlinearity (DNL) specifies the uniformity of a converter's bit width. In a "perfect" A/D converter, each code would be precisely 1 LSB wide; that is, the range of voltages that would yield a given output code would, ideally, be exactly the full-scale voltage divided by the resolution (number of codes, or 2^n) of the n-bit ADC. DNL therefore is typically specified as fractions (or multiples) of an LSB; ±½ or ±1 LSB are commonly specified values.

Note that it's possible for an A/D converter to have DNL of almost 2 LSBs in the positive direction, but no more than 1 LSB in the negative direction. Positive DNL indicates codes that are too wide, whereas negative DNL indicates codes that are too narrow. Negative DNL can be at worst −1 LSB for any code; at that extreme value, the code ceases to exist. In order for an ADC to have n bits of true resolution, all 2^n codes must exist; therefore, negative DNL must never exceed −1 LSB.

Some applications, however, require not only that all

Scientific conversions place tough demands on ADCs

Large-scale experiments require many channels of data acquisition. The Time Projection Chamber of SLAC (Stanford Linear Accelerator Center), for example, has approximately 17,000 channels of 9-bit resolution. The system for the LEP (large electron positron) experiment at CERN (European Center for Nuclear Research) will have 50,000 channels, and experiments at Fermilab may require as many as 100,000. Historically, the Wilkinson run-down (single-slope) ADC architecture has been adequate for applications such as these, both for its simplicity and its excellent differential nonlinearity or uniformity of bit width.

However, all such slope-conversion ADCs are slow, because the conversion process is basically a linear search through the range of all possible discrete values. Conversion of a full-scale input takes 2^n steps, where n is the resolution of the ADC. In order to achieve reasonable conversion times, slope-conversion ADCs either sacrifice resolution or run at extremely high clock rates. The problems of dealing with 100-MHz clocks on an analog board can substantially complicate the basic simplicity of slope-conversion ADCs.

One way to obtain high-speed, high-resolution converters is to use a successive-approximation algorithm to control a D/A converter. Converters of this type are fast because they perform a binary search of all possible discrete values, so that regardless of input amplitude, conversion takes n clock times.

Take your pick

A number of manufacturers offer complete ADCs that use this conversion technique. In hybrid form, 12-bit ADCs having conversion times of 1 to 10 μsec cost $400 to $100; the faster ADCs are, of course, more expensive. Monolithic 12-bit ADCs with conversion times of 5 to 15 μsec and in the $30 to $100 price range are also available.

The advent of these low-cost, high-performance integrated ADCs allows you to construct A/D-conversion systems that have either a very fast ADC in each channel or cost-effective, multiple-channel, time-shared ADCs. Integrated successive-approximation ADCs offer low cost, high speed, and good resolution, but it's important to ascertain if they are good enough for exacting scientific applications.

The main objections to using integrated successive-approximation converters in critical applications are inadequate speed and DNL. To make effective use of an ADC in a time-shared, multiple-channel system, you often need a conversion time on the order of 5 μsec, or even less. Further, such applications as spectroscopy require DNL of approximately 1% of an LSB, to ensure that the measured spectrum accurately represents the statistics of the process being studied rather than the statistics of the ADC being used for the measurement.

Successive-approximation ADCs in general, whether hybrid or monolithic, have trouble with DNL for two main reasons. First, insufficient settling time can lead to wrong bit choices. For the most basic implementation of a successive-approximation ADC, every bit, including the MSBs, must settle to LSB accuracy in order to guarantee correct results.

Second, because any code is the summation of n different sources, each with its own inaccuracy, bit width is not uniform. Technically and economically successful use of integrated ADCs in critical applications requires the minimization of conversion time and DNL, as well as minimization of the required support circuitry.

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One way of achieving tight bit-width uniformity for scientific applications requiring good differential linearity is through calibration and software.

possible codes exist, but also that they be of uniform size; spectroscopic or histogramming applications are prime examples (see **box,** "Scientific conversions place tough demands on ADCs"). As a physical analogy, consider the analog input to be in the form of small pellets fired from a gun and having a certain average velocity, and the A/D converter to be an open box having equally spaced partitions into which these pellets come to rest. By counting up the number of pellets in each partition, it's possible to reconstruct the velocity distribution of the gun.

If the partitions in the box aren't equally spaced, then the pellet count per partition no longer reflects the statistics of the process being measured but rather the combination of the process statistics and the measurement device's statistics. This analogy is very close to the problems encountered in nuclear-pulse measurement, where tens or hundreds of thousands of events are digitized and sorted by amplitude to yield an energy spectrum. ADCs characterized for these applications must have DNLs of 1% of an LSB or better.

One way of achieving this tight bit-width uniformity for histogramming applications is simply through calibration and software. In principle, you can characterize an ADC by using an input signal (whose characteristics you know to a high degree of accuracy) such as a linear ramp or sine function. You can then compare the accumulated counts per code against expected values and construct a correction table, giving multiplication constants for each code to correct for the over- or underabundance of events recorded for each code.

This calibration method relies on the stability of the imperfections in the system in order to work. Count-rate dependence, power-supply sensitivity, and component drift can easily combine to render this baseline calibration useless. Periodic recalibration can help, but this method will always require significant off-line computational resources.

Hardware methods improve ADCs

Three basic hardware techniques can improve DNL or reduce conversion time:

- Progressive clocking
- Gatti method (sliding scale)
- Error correction.

Progressive clocking takes advantage of the fact that for successive-approximation ADCs, bit-decision time consists of the logic delay plus the internal D/A converter's settling time. The logic delay is fixed, but the DAC's settling time depends on the bit being switched—MSBs take longer to settle to LSB accuracy than do LSBs. Progressive clocking allows more time for the MSBs to settle and speeds up the bit-decision times for the LSBs.

In the ideal case, each bit is allotted only as much time as it actually needs to make a correct decision, rather than the full MSB-decision time. The result of a progressive-clocking scheme is to give better DNL at any given conversion time, or to allow you to use faster conversion times before the ADC drops codes. In practice, using just two clock speeds offers substantial benefits over using a constant-rate clock.

This analysis evaluates the effectiveness of progressive clocking in permitting shorter conversion times. The ADC of choice is the Am6112, a monolithic 12-bit ADC with a guaranteed fixed-clock conversion time of 10 μsec and a 4-σ distribution point of 8.6 μsec (99.995% of parts will achieve this conversion rate). The Am6112 is a microprocessor-compatible ADC that has five operating modes: two triggered by the ADC's $\overline{\text{RD}}$ input, two triggered by the $\overline{\text{WR}}$ input, and one stand-alone mode triggered by the coincidence of $\overline{\text{RD}}$ and $\overline{\text{WR}}$.

The basic Am6112 application circuit uses the stand-alone mode and a fixed clock frequency; a 74LS164 shift register and a few inverters perform all necessary timing and control functions. You can easily modify this basic circuit to provide a 2-speed progressive clock by adding a few flip-flops and gates to provide both the f and 2f clocks and the means to switch between them (**Fig 1**). Using this simple setup, you obtain best results by switching from the f to the 2f clock after 7.5 clock periods (bit 5); the result is a 20% reduction in minimum conversion time.

Reduce clock time bit-by-bit

You can obtain additional improvements in conversion time by varying the clock at each bit, allowing only as much settling time as the converter actually needs for each bit decision. You can easily achieve this bit-by-bit clock modulation by configuring PROMs as microprogrammed state machines in which the correct clock width for each bit depends on the number of ones and zeros programmed into the PROM. **Fig 2** shows an example of this technique using Am27S25 registered PROMs.

Data bits D_0 through D_5 on PROM IC_1 generate the necessary control signals for the Am6112 ADC, the sample/hold amplifier, and the output registers. The remaining PROM data bits serve to supply next-address information for the state machine. The PROMs allow

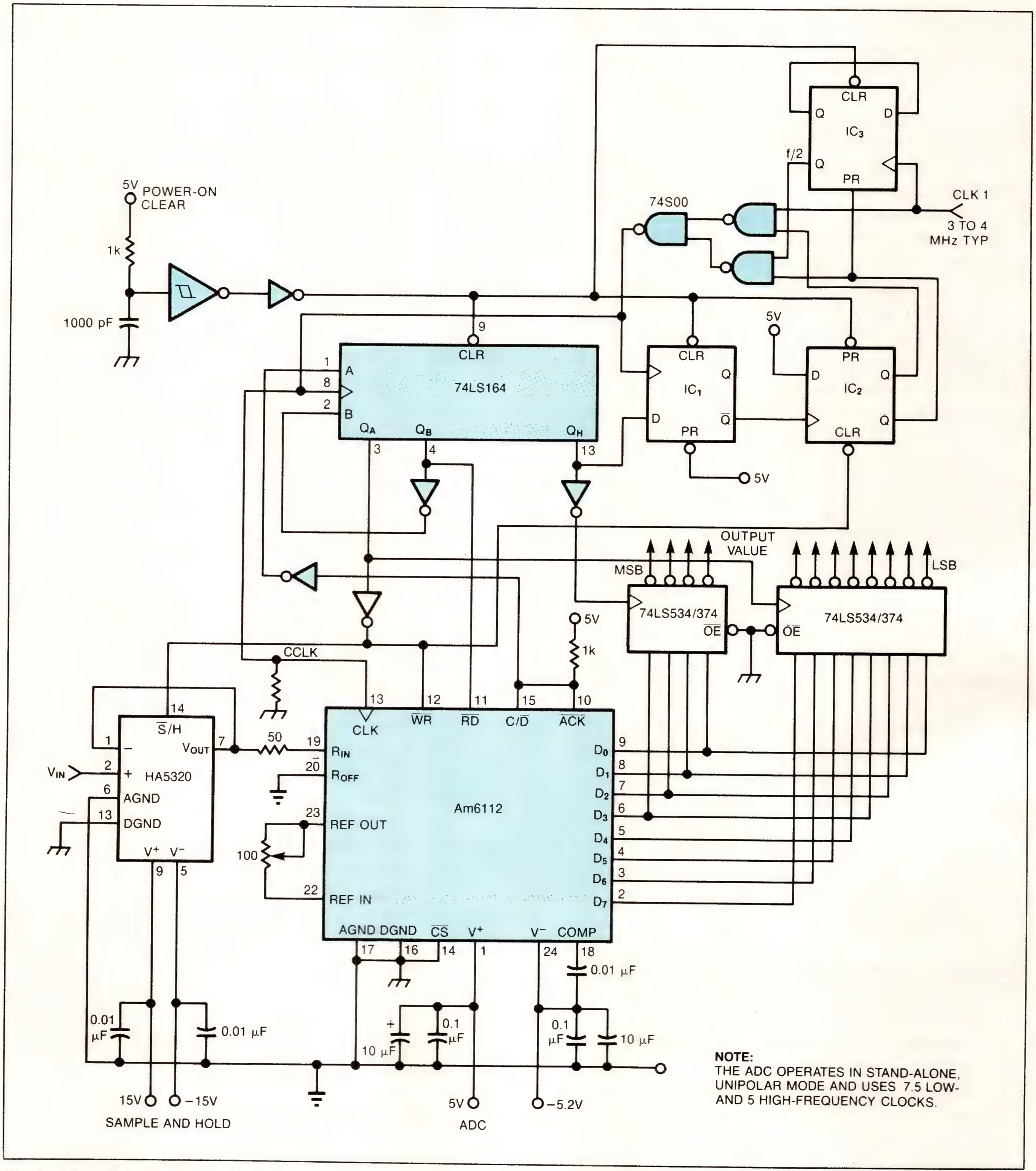

***Fig 1—A 2-step progressive clock** improves the conversion speed of the Am6112 12-bit, monolithic A/D converter by 20%. The clock frequency doubles after the determination of bit 5 in the successive-approximation process.*

Progressive clocking relies on the fact that an ADC's internal DAC settles faster for the less significant bits under determination by the successive-approximation process.

direct implementation of any desired timing sequence; the ADC's clock width is set by the number of ones and zeros in successive PROM locations. For a 50% ADC-clock duty cycle, you must drive the state machine with a clock whose frequency is twice the highest ADC-clock frequency. For example, for a 2-speed progressive clock having f=2 MHz and 2f=4 MHz, you must drive the PROMs at 8 MHz.

The Am6112 is primarily intended for direct connection to a microprocessor bus. Depending on the mode chosen, $\overline{RD}$ or $\overline{WR}$ can trigger conversions. In the case of an Am6112 that interfaces to a microprocessor, you must synchronize the progressive-clock generator to the start-conversion signal to ensure that the clock frequency changes at the correct bit decision. **Fig 3** shows a typical Am6112-microprocessor setup that uses an Am27S25 registered PROM as a progressive-clock generator.

In mode 0, $\overline{WR}$ triggers the Am6112. $\overline{CS}$ and $\overline{WR}$, gated together, clear the register inside the Am27S25, resetting the state machine to address 0. This operation synchronizes the state machine to the conversion cycle of the Am6112. The PROM is programmed to "stop" after conversion is complete. Programming an address value equal to the last-address value in the last-address-value location causes the state machine to "stick" at this location.

You can achieve more sophisticated bit-by-bit timings by using only the minimum clock-high time and setting the PROM clock to a multiple of the desired detent (incremental bit time). Results obtained using careful bit-by-bit timing show a 40% reduction in conversion time as compared with that of a standard, fixed-clock circuit.

Compare variable-clock DNLs

You can produce plots of DNLs by feeding a very pure sine wave to the converter under test (the Am6112), via a Harris 5320 sample/hold amplifier. The ADC is allowed to free-run; its output from each conversion increments the contents of an address in a histogramming memory. When a location overflows, the conversion stops and the computer (in this case an H-P 9825) reads out the histogramming memory. Software in the computer corrects for the probability density of the sine function and plots these corrected

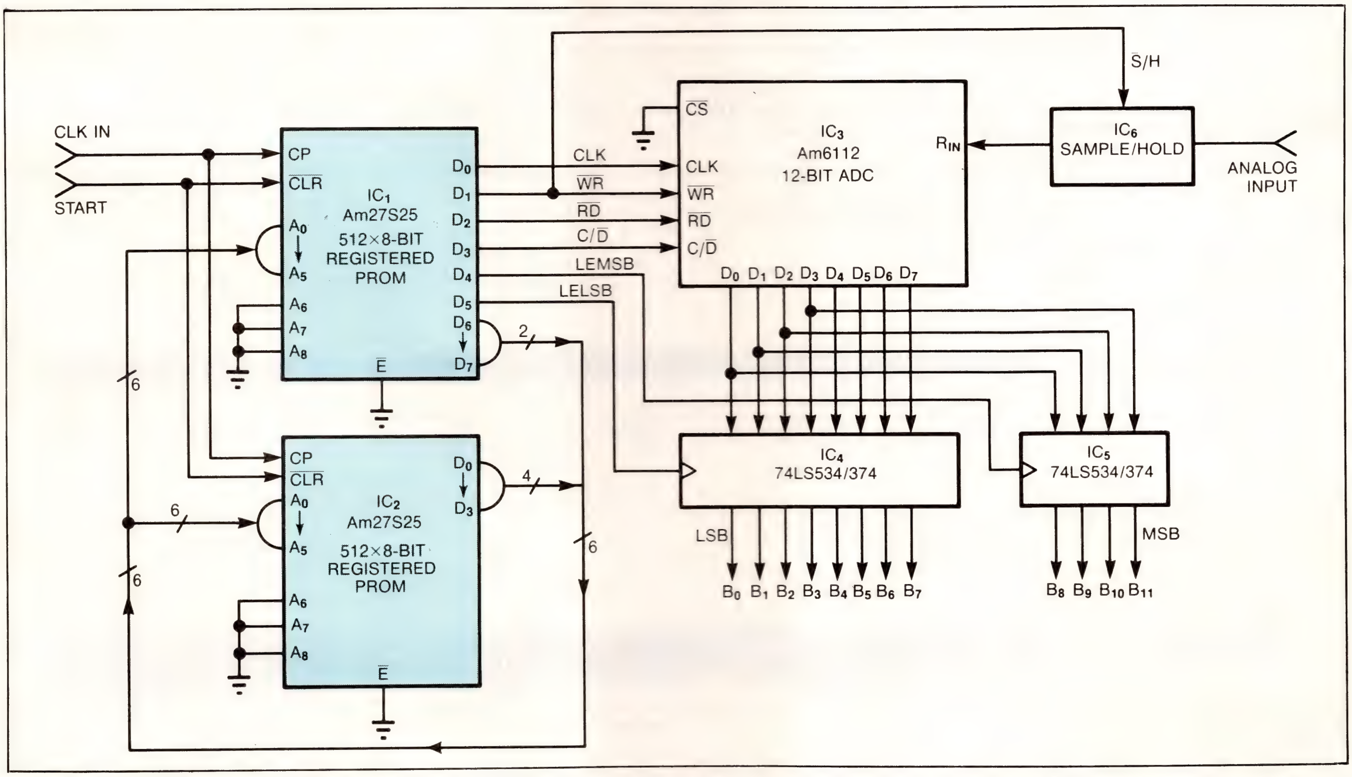

***Fig 2—Registered PROMs provide bit-by-bit progressive clocking** in this circuit configuration. The PROMs are microprogrammed state machines that determine the correct clock width for each bit in the conversion process.*

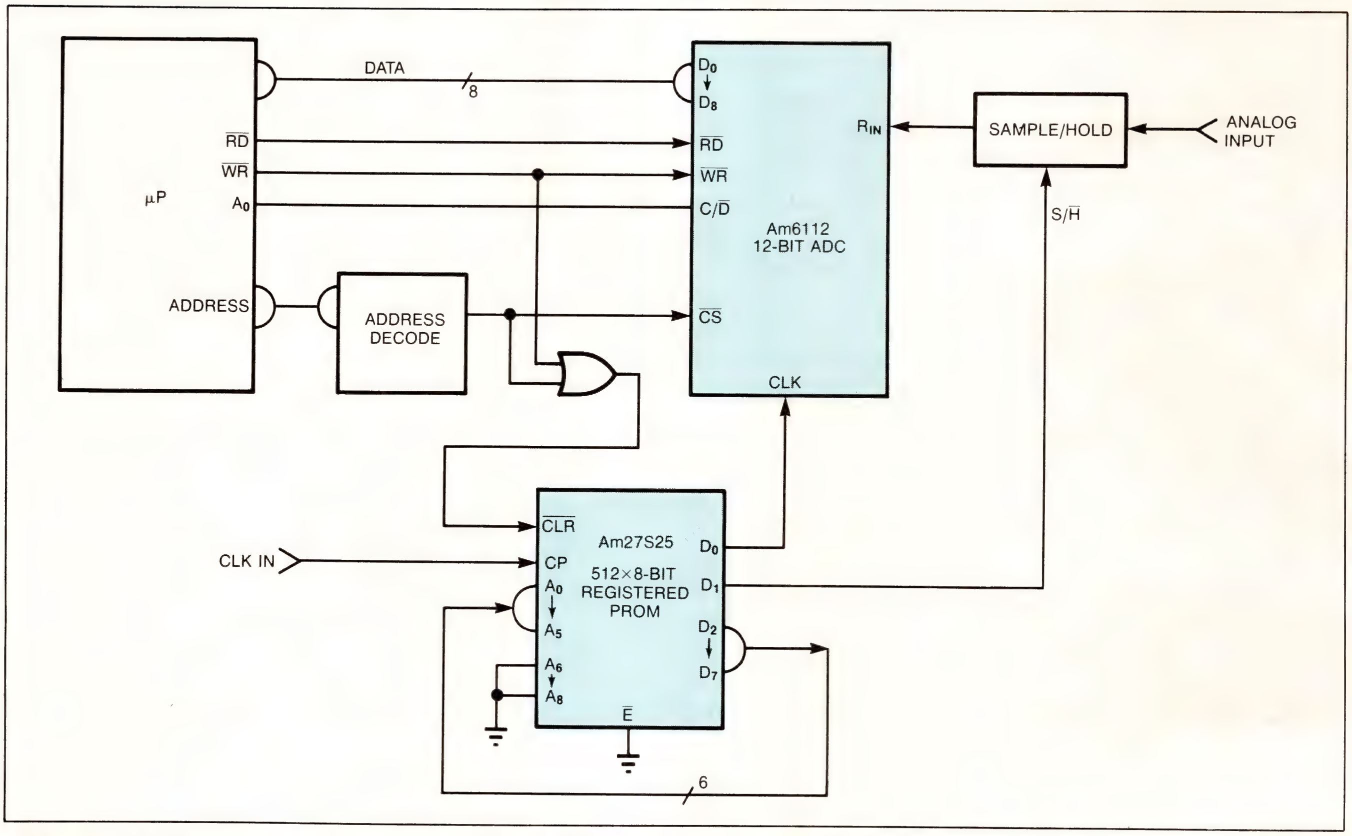

***Fig 3—Bit-by-bit progressive clocking cuts conversion time by 40%** in this microprocessor-based A/D-conversion system. A PROM provides the correct clock width to the A/D converter for each bit decision.*

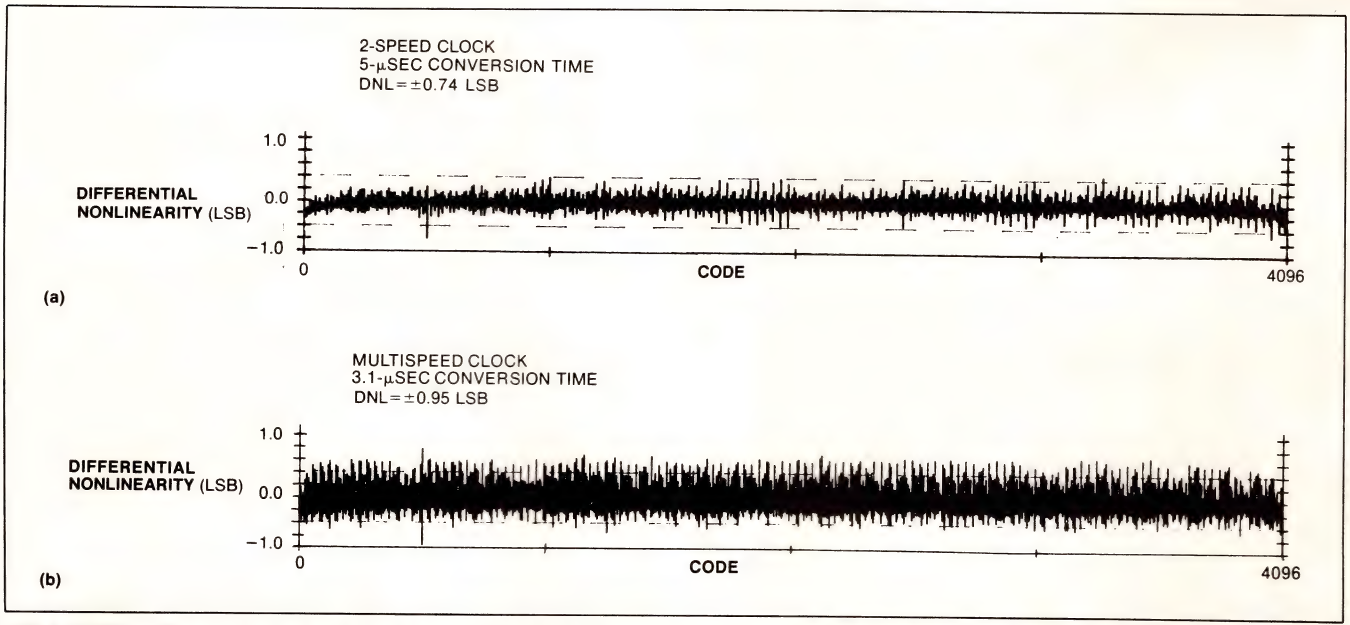

***Fig 4—Differential nonlinearity is within acceptable limits** for these results obtained by using progressive clocking to accelerate an Am6112 A/D converter. In **a,** a 2-speed clock drives the ADC; in **b,** a variable clock controls each bit time individually.*

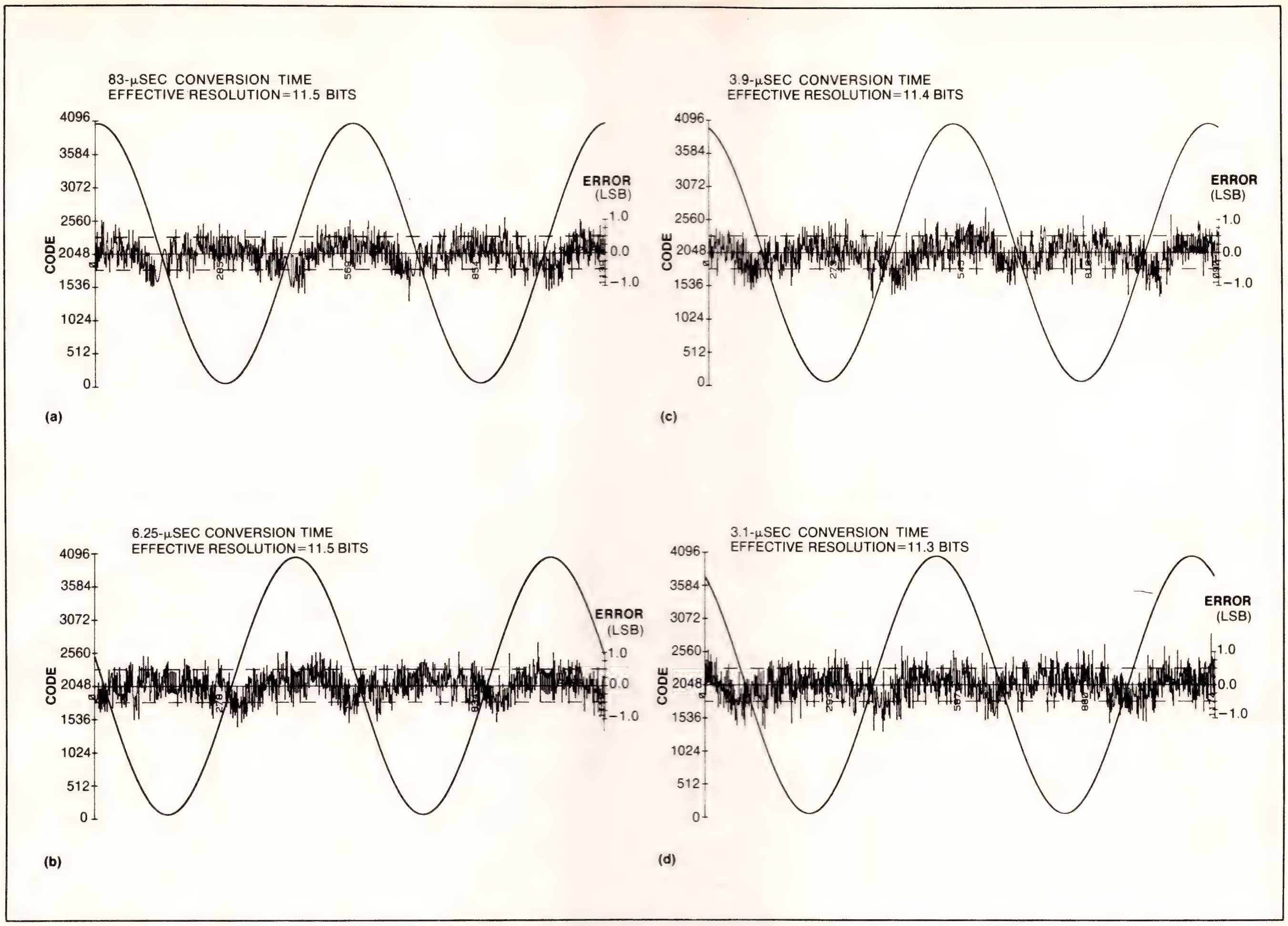

Fig 5—Effective-resolution plots illustrate an ADC's performance. A fixed-rate clock drives the converter in ***a*** *and* ***b;*** *2-speed and multispeed clocks determine the ADC's speed in* ***c*** *and* ***d,*** *respectively. Corresponding conversion times for the four clocking methods are 83, 6.25, 3.9, and 3.1 μsec. The effective resolution is substantially the same for all four clocking schemes.*

counts per code as differential nonlinearity.

Fig 4a shows DNL for an Am6112 driven by a 2-speed clock with a conversion time of 5 μsec (vs the standard 8.6 μsec). You can achieve even better results by controlling each bit time individually. **Fig 4b** shows the same part running at a 3.1-μsec conversion time, yet still having better than ±1-LSB DNL. The 2-speed clock uses the modified basic application circuit.

The multispeed clocks come from an HP word generator, although practical instruments need only use a couple of PROMs, as described earlier. Note that for the Am6112, the settling time for the MSB−1 is almost as severe as the MSB's settling time because the MSB is allotted 1.5 clock times to settle; all other bits are given only one clock time.

An effective-resolution test assesses the overall performance of the Am6112 using various clocking schemes. In the effective-resolution test, the ADC digitizes an almost-full-scale sinusoid. The computer then uses least-square-error minimization techniques to fit an idealized sinusoid to the data. The idealized sinusoid is of the form $A\cos(2\pi ft+\theta)+dc$, where the amplitude, frequency, phase, and dc offset are iteratively calculated to best fit the digitized data.

The actual rms error includes errors caused by quantization, differential nonlinearity, integral nonlinearity, sample/hold-amplifier aperture jitter, noise, and missing codes. You can calculate the effective number of bits from this actual rms error. The computation is of the form

$$\text{effective bits}=n-\log(\text{actual rms error}/\text{ideal rms error}),$$

where n is the number of bits the converter can accommodate.

The four effective-resolution plots of **Fig 5** show the improvements in overall system performance made possible by using progressive-clocking techniques. Each plot shows the digitized input (sine wave) and also the residual error from the ideal sine wave. The first plot **(Fig 5a)** shows the results obtained by using a constant 66-kHz clock, corresponding to 83-μsec conversion time. This plot is a reference plot; it reflects the same conditions as those of the automated factory test.

The next plot **(Fig 5b)** shows that a 2-MHz constant clock (6.25-μsec conversion time) produces the same result as that obtained by using the slower, automated factory test; that is, good correlation exists. The third plot **(Fig 5c)** shows the almost 40% reduction in conversion time (to 3.9 μsec with essentially identical effective resolution) you can obtain by using a 2-speed progres-

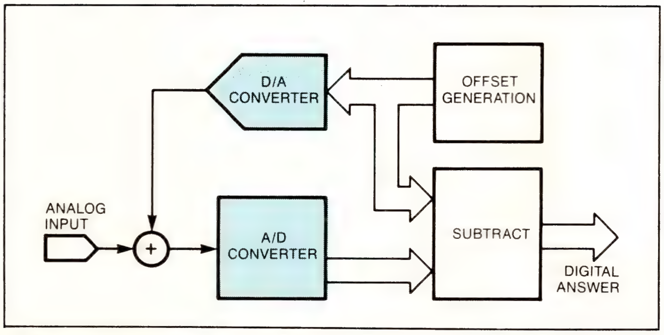

***Fig 6—A method to ensure bit-width uniformity,** or low differential nonlinearity, the Gatti sliding-scale technique adds an offset voltage to an A/D converter's input, then subtracts the offset digitally from the ADC's output.*

sive clock. The final plot **(Fig 5d)** shows the additional reduction in conversion time (to 3.1 μsec) you can realize by using a fully progressive clock.

The Gatti, or sliding-scale, technique is another scheme for ensuring bit-width uniformity. This method adds in a random analog offset at each conversion and digitally subtracts the offset at the output **(Fig 6).** In this way, over a large number of conversions, the ADC exercises all codes within the range of the offset, averaging the difference in bit width over the entire offset range. If you choose a 6-bit offset, then the DNL of any bit is reduced by a factor as great as 64. The technique, although simple and powerful, has certain caveats you should be aware of.

The offset is not free, in the sense that it comes directly out of the dynamic range the converter spans. For the cited 6-bit offset, the method would render 64 codes unusable—either 64 at the top end or 64 at the bottom end of the ADC's dynamic range. However, for a 12-bit converter having 4096 codes, the loss of 1/64th of the possible dynamic range often isn't significant.

The way you choose analog offsets for each conversion is important; the basic rule is, the more random the better. The simplest offset selection entails the use of a counter. However, if the counter's period is harmonically related to that of the input signal, results could be especially bad, as the ADC could exercise particular codes repeatedly over the entire offset range and thereby defeat the desired averaging effect. A safe form of offset selection uses a pseudorandom shift-register circuit (shift register and exclusive-OR feedback) to prevent the inadvertent synchronization of the input and offset signals.

A more serious limitation of the Gatti method is that the technique won't correct for uncertainty in the

LISTING 1—SIMULATION ROUTINE FOR ADC

```
10 REM A/D EMULATION
12 REM STEVEN SIDMAN 4/29/86
13 REM SHOWS EFFECTS OF IMPERFECT BIT
14 REM WEIGHTS AND COMPARATOR UNCERTAINTY
15 OPEN4,4:REM ENABLE PRINTER
20 DIM D(8):DIM V(256):DIM Q(5)
25 FOR I=0TO255:V(I)=0:NEXTI
30 REM ASSIGN IMPERFECT BIT WEIGHTS
40 FOR I=0TO7:READD(I):NEXTI
50 DATA .809665988,2.09582035
55 DATA 4.21482403,7.87046019
60 DATA 16.0982544,32.1535335
65 DATA 63.9183358,128.221066
70 REM INITIALIZE OFFSET REGISTER
80 FOR I=0 TO 4:Q(I)=0:NEXT I
110 REM INPUT RAMP SIGNAL
120 FORI=0TO255*25:RP=I/25
122 REM GOSUB 2000:REM ASSIGN GATTI OFFSET
125 REM RP=RP+O
130 GOSUB1010:REM A/D CONVERSION ROUTINE
140 REM CODE=CODE-O
150 V(CODE)=V(CODE)+1:REM BUILD HISTOGRAM
155 NEXTI
180 REM:FOR I=0TO7:PRINT#4,"BIT ";I,"VALUE ";D(I):NEXT
190 PRINT#4:PRINT#4
200 FOR I=0TO255
210 PRINT#4,"CODE ";I;"COUNT";V(I)
220 NEXTI
225 CLOSE4
230 END
1000 REM A/D CONVERSION SUBROUTINE
1001 REM SOFTWARE EMULATION OF SUCCESSIVE
1002 REM APPROXIMATION. LINE 1017 EMULATES
1003 REM COMPARATOR UNCERTAINTY FOR EACH
1004 REM BIT DECISION
1010 SUM=0:CODE=0
1015 FORK=7TO0STEP -1
1017 X=RP+(.5-RND(1))
1020 IFX)(SUM+D(K))THEN CODE=CODE+(2↑K)
1030 IFX)(SUM+D(K))THEN SUM=SUM+D(K)
1040 NEXT K
1050 RETURN
2000 REM GATTI
2002 REM LINES 10-60 FORM EXOR OF Q4&Q3
2004 REM LINES 70&80 INVERT FOR XNOR
2006 REM LINES 90-130 IMPLEMENT SHIFT
2007 REM REGISTER FOR 5 BIT PRBS
2008 REM LINES 150-180 USE CURRENT PRBS
2009 REM VALUE FOR OFFSET
2010 A=Q(4):B=Q(3)
2020 IF A=1 THEN NA=0
2030 IF A=0 THEN NA=1
2040 IF B=1 THEN NB=0
2050 IF B=0 THEN NB=1
2060 T1=(A AND NB)OR(B AND NA)
2070 IF T1=1 THEN NT=0
2080 IF T1=0 THEN NT=1
2090 FOR G=4 TO 1 STEP -1
2100 Q(G)=Q(G-1)
2120 NEXT G
2130 Q(0)=NT
2140 REM FORM OFFSET VALUE
2150 O=0
2160 FOR G=0 TO 4
2170 O=O+(Q(G)*(2↑G))
2180 NEXT G
2190 RETURN

READY.



READY.
```

Instead of using a 2-speed clock, you can improve conversion time by varying the clock at each bit, allowing only the time the converter needs for each bit decision.

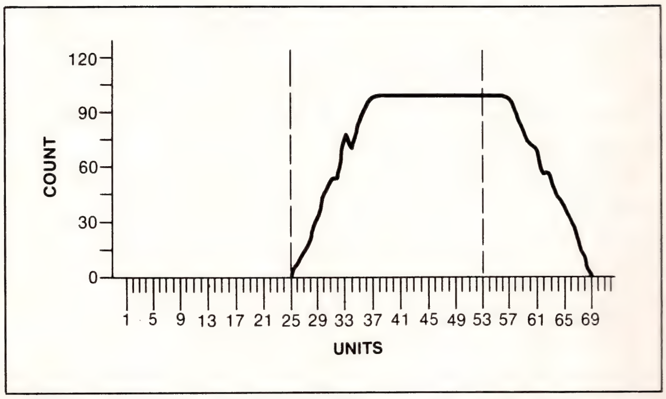

Fig 7—The result of using a nonideal DAC and a nonideal comparator in an ADC, *this channel profile uses the Basic ADC-emulation program of* ***Listing 1.***

comparator. It corrects (for a large number of samples) only for imprecise matching in the bit weights of the DAC that reconstructs the amplitude of the analog signal being measured. If you use the technique in an attempt to create uniform code widths in an ADC that exhibits large comparator uncertainty, the result will be a converter in which all codes exist and have uniform width, but whose code widths will exceed an LSB for all codes. Codes in this case will no longer be distinct but will overlap with neighboring codes, rendering the sliding-scale-corrected ADC just as unfit for spectroscopic work as an unmodified ADC.

You can obtain some insight into the effects of nonideal circuit blocks in an A/D converter by constructing a software model of an ADC **(Listing 1),** varying

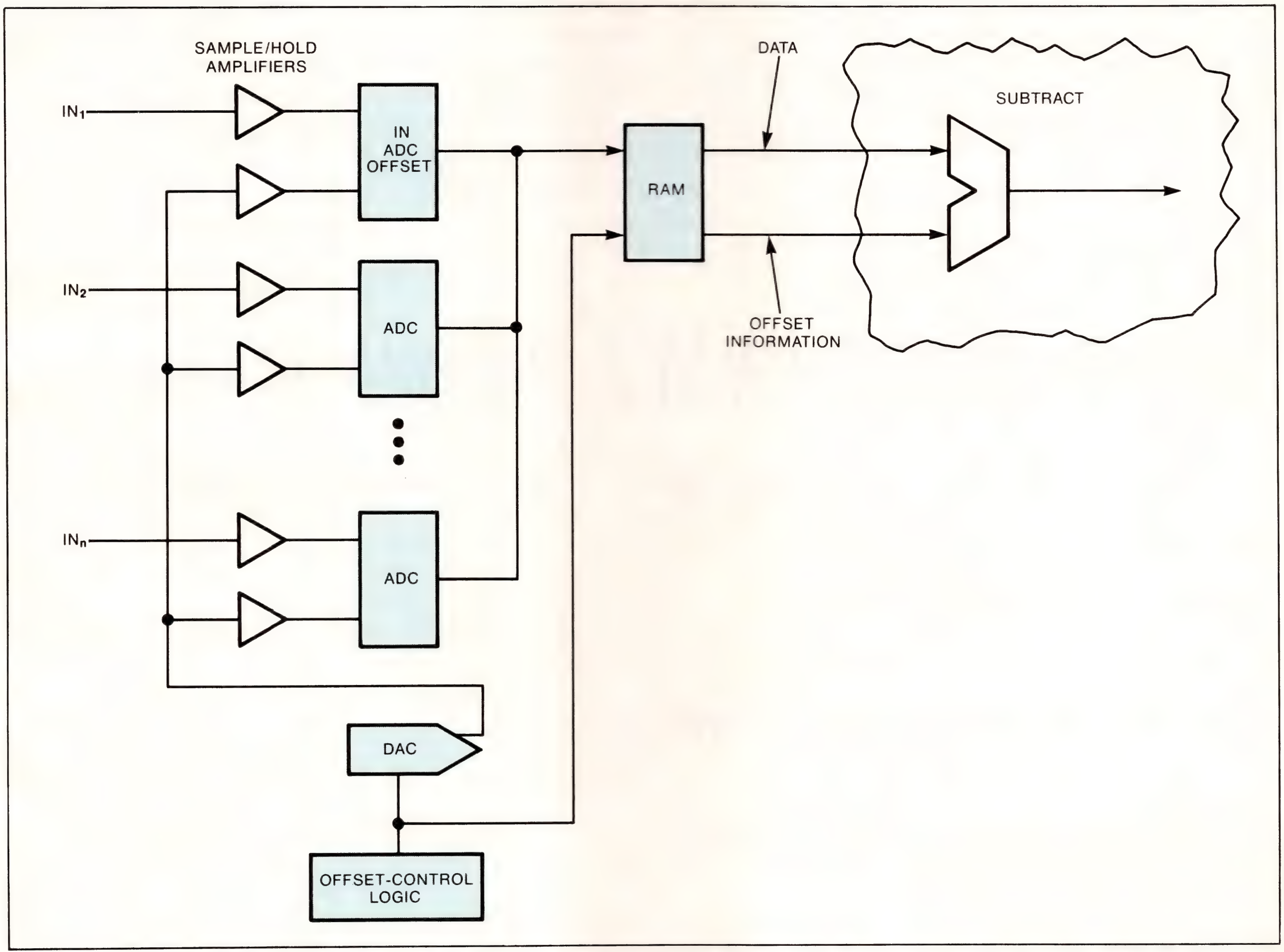

Fig 8—You can use the Gatti technique with multichannel A/D-conversion systems, *as this configuration shows. The offset D/A converter and much of the control logic are common to all the A/D converters. The RAM holds the common-offset information for the required subtraction operation.*

The Gatti method adds a random analog offset at each conversion and digitally subtracts the offset at the output.

relative bit weights from the ideal of exact powers of 2, and providing for various levels of uncertainty in the comparator. With an ideal DAC and an ideal comparator, the channel profile (the plot of output codes vs the input voltages that produce those codes) will be perfectly rectangular.

In essence, the probability of a code being asserted is 100% for all voltages within the span of that code and 0% elsewhere. A nonideal DAC and an ideal comparator will result in abnormally wide or narrow channel profiles, which in fact may not be continuous for any given code. Some codes simply may not exist. An ideal DAC and a nonideal comparator will yield a channel profile whose sides are sloped and extend into adjacent codes by the amount of the comparator's uncertainty.

For example, a comparator having ½ LSB of uncertainty will give a triangular shape to the profile, with the apex corresponding to the mid-code voltage and the bottom vertices extending halfway into the adjacent codes. A nonideal DAC and a nonideal comparator will give a channel profile **(Fig 7)** that has the same basic spread as the nonideal-DAC case but that is smoothed over by the "dither" of the comparator's uncertainty. Indeed, codes that wouldn't exist at all because of the addition of imprecise DAC bit weights are now possible because the comparator will occasionally make a "wrong" decision.

The sliding-scale technique can ensure uniform code widths for those cases where the statistics of a signal are of more interest than the time-ordered history of that signal. The intended applications for the technique are more dependent on histograms than on signal reconstruction. In addition, the Gatti method can't ensure that each code is only 1 LSB wide. Assuming the DAC is allotted sufficient settling time, the code width is governed by the comparator's uncertainty.

A final limitation of the sliding-scale technique is that it will work only with linear-scale ADCs. The technique works because every bit is assumed to be 1 LSB wide. This assumption isn't valid for logarithmic or other nonlinear-scale A/D converters, which are suitable whenever dynamic range is more important than resolution. Often, high linear resolution is required merely to obtain a dynamic range that will encompass all

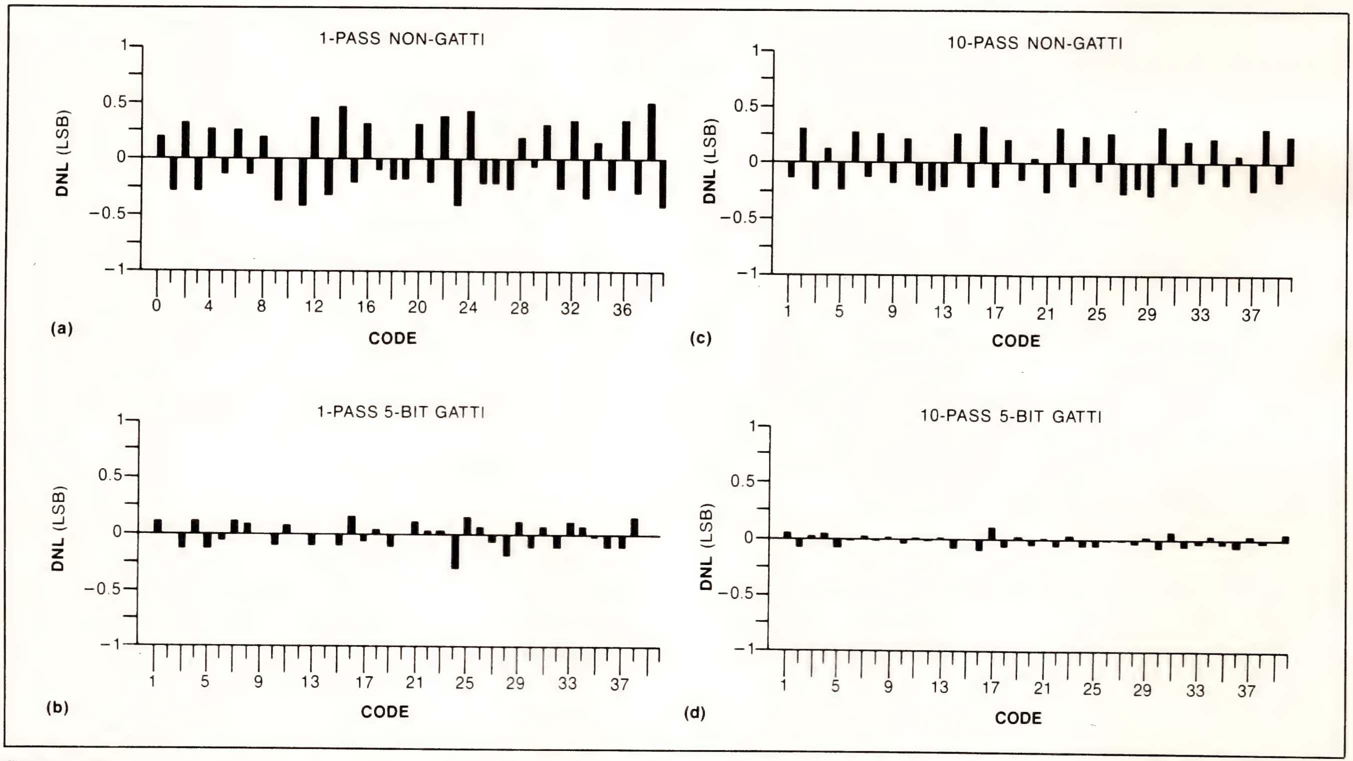

Fig 9—These plots show the simulation results *for different ADCs using and not using the Gatti method. The plots show differential nonlinearity as a function of code weight. In* ***a,*** *the non-Gatti ADC has incorrect DAC bit weights and comparator uncertainty;* ***b*** *shows the results of applying the Gatti method. Averaging over 10 passes* ***(c)*** *improves DNL somewhat in the non-Gatti ADC;* ***d*** *shows the improvement for 10-pass averaging when you apply the Gatti method.*

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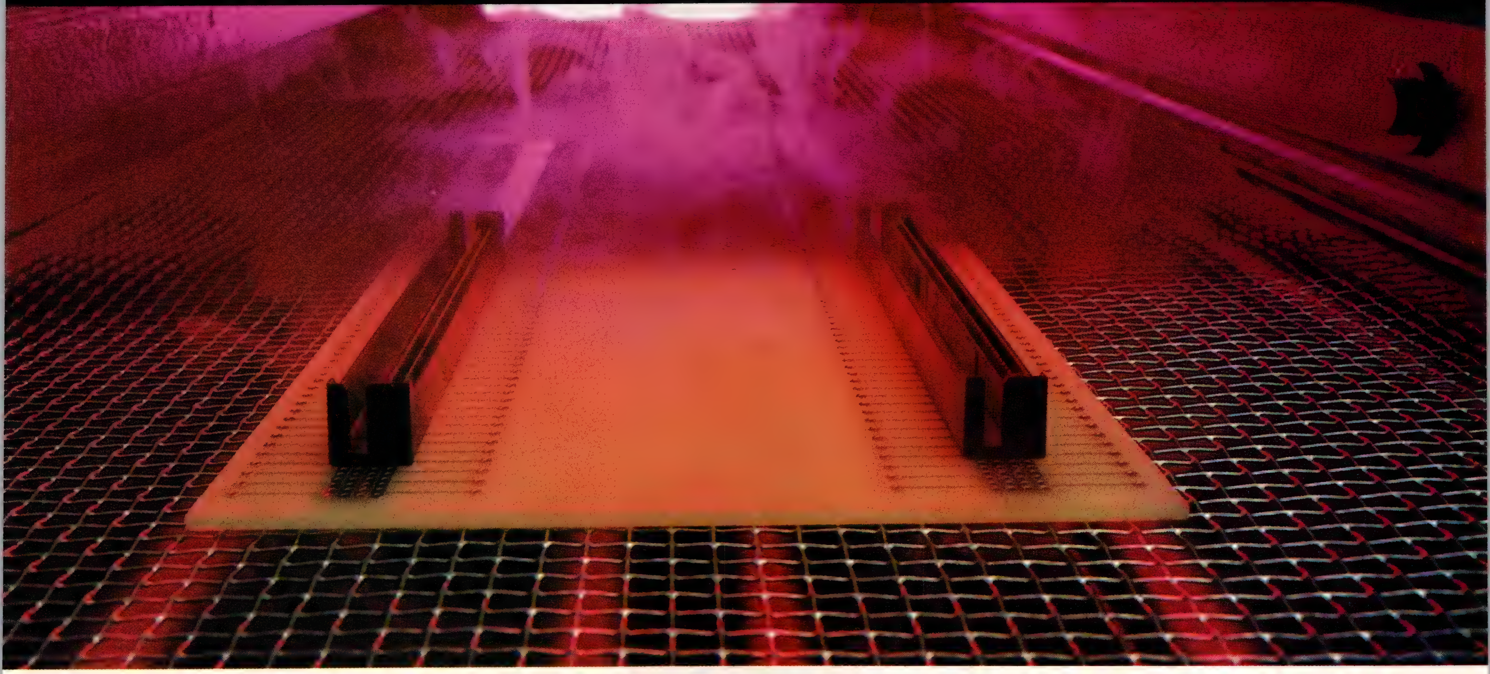

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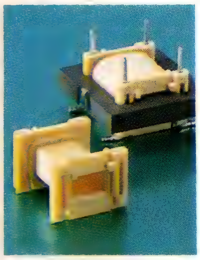

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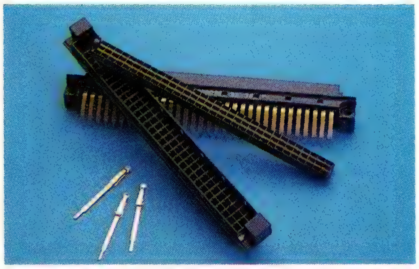

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The sliding-scale technique can ensure uniform code widths for cases where the statistics of a signal are of more interest than the time-ordered history of that signal.

anticipated events. For example, particle identification requires a resolution of perhaps 1 part in 10 at any given energy, but the range of energies can be 256 to 1 or greater.

A nonlinear converter is one for which the dynamic range is not the same as the resolution. A nonlinear solution allows you to use a less complex converter to perform a given job by putting the accuracy in that part of the range where it is really needed. A common application of nonlinear conversion is in the codecs used in telecommunications, where 8-bit devices provide 11 bits of dynamic range. Because the adjacent codes in these converters are, by definition, not of equal width, you can't apply the Gatti method.

The method is well suited to applications that require many channels of data acquisition, as the offset DAC and much of the digital hardware can be common to a large number of ADCs. The suggested configuration shown in **Fig 8** illustrates this concept; here, multiple sample/hold amplifiers, driven by one DAC, introduce

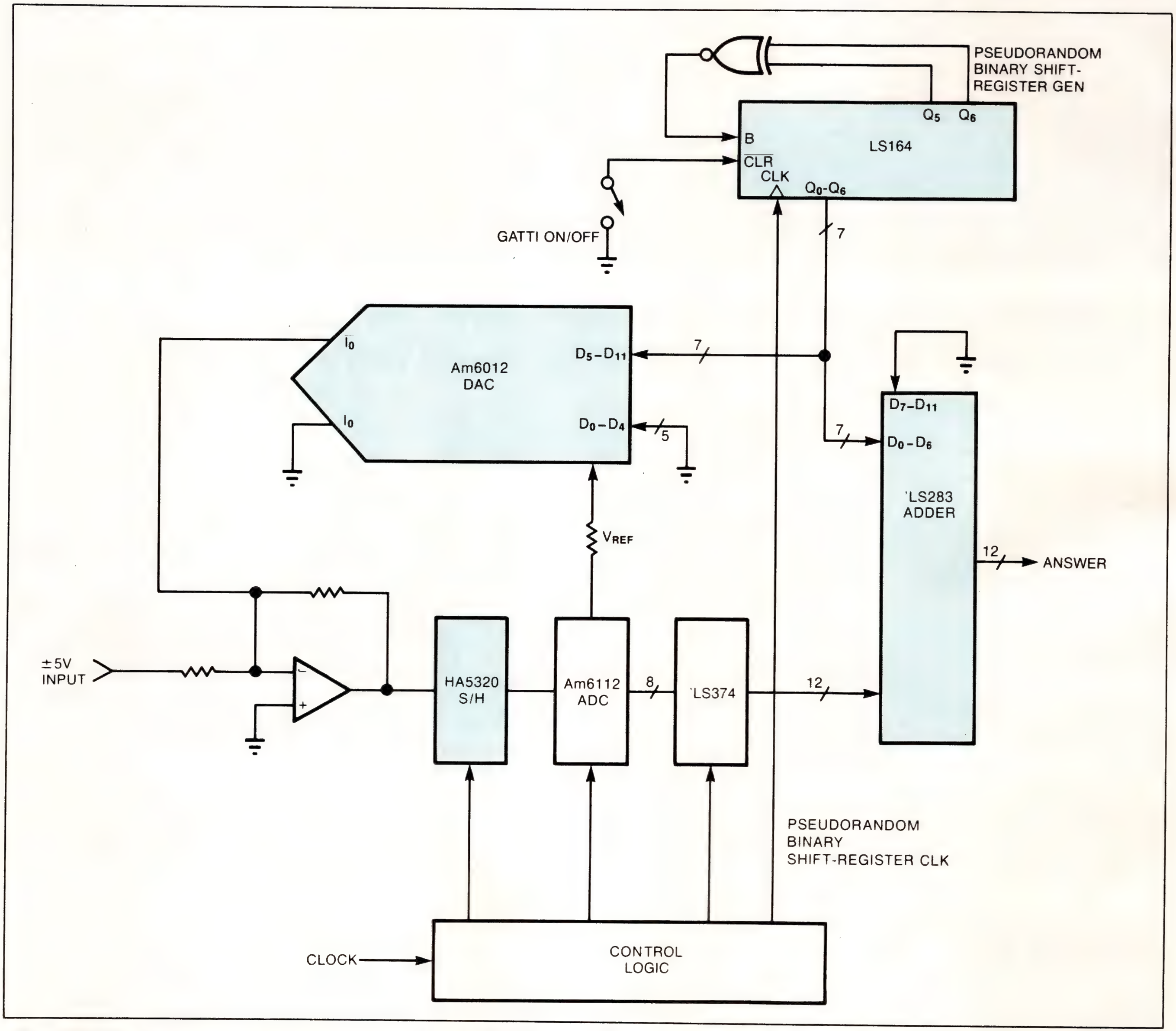

Fig 10—In this demonstration circuit, *the circuit blocks necessary for implementing Gatti sliding-scale DNL improvement are an offset D/A converter, a sample/hold amplifier, a 7-bit pseudorandom binary shift register, and three 4-bit adder chips.*

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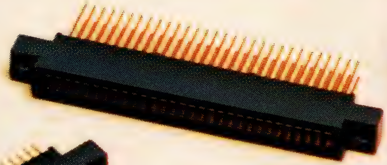

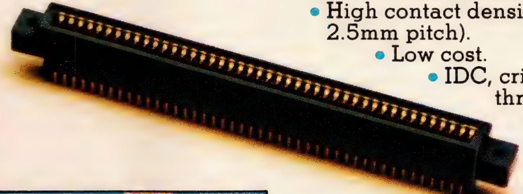

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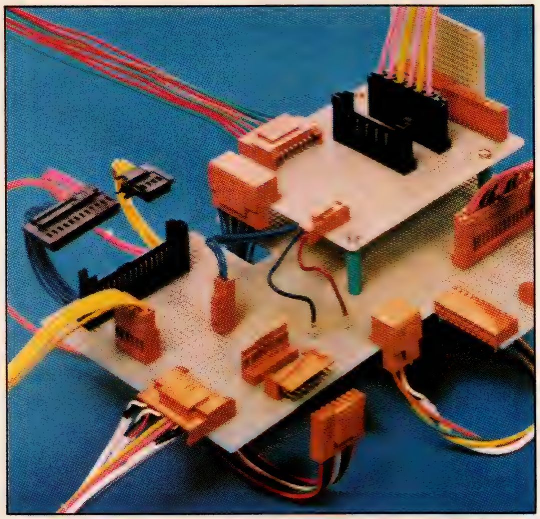

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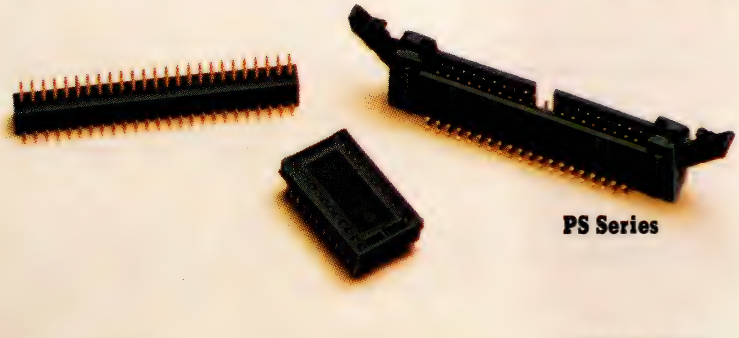

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The improvement the Gatti method makes in the DNL of a deliberately nonideal ADC is evident in the simulation results of **Fig 9.** The input to the ADC is a very slow ramp, and 25 conversions contribute to each code count. **Fig 9a** shows the DNL of the raw ADC; here, the variations result from the imperfect bit weights and the random comparator uncertainty. **Fig 9b** shows the effect of using the Gatti technique under the condition of a single occurrence of a slow ramp input.

Fig 9c shows the DNL of a non-Gatti ADC for 10

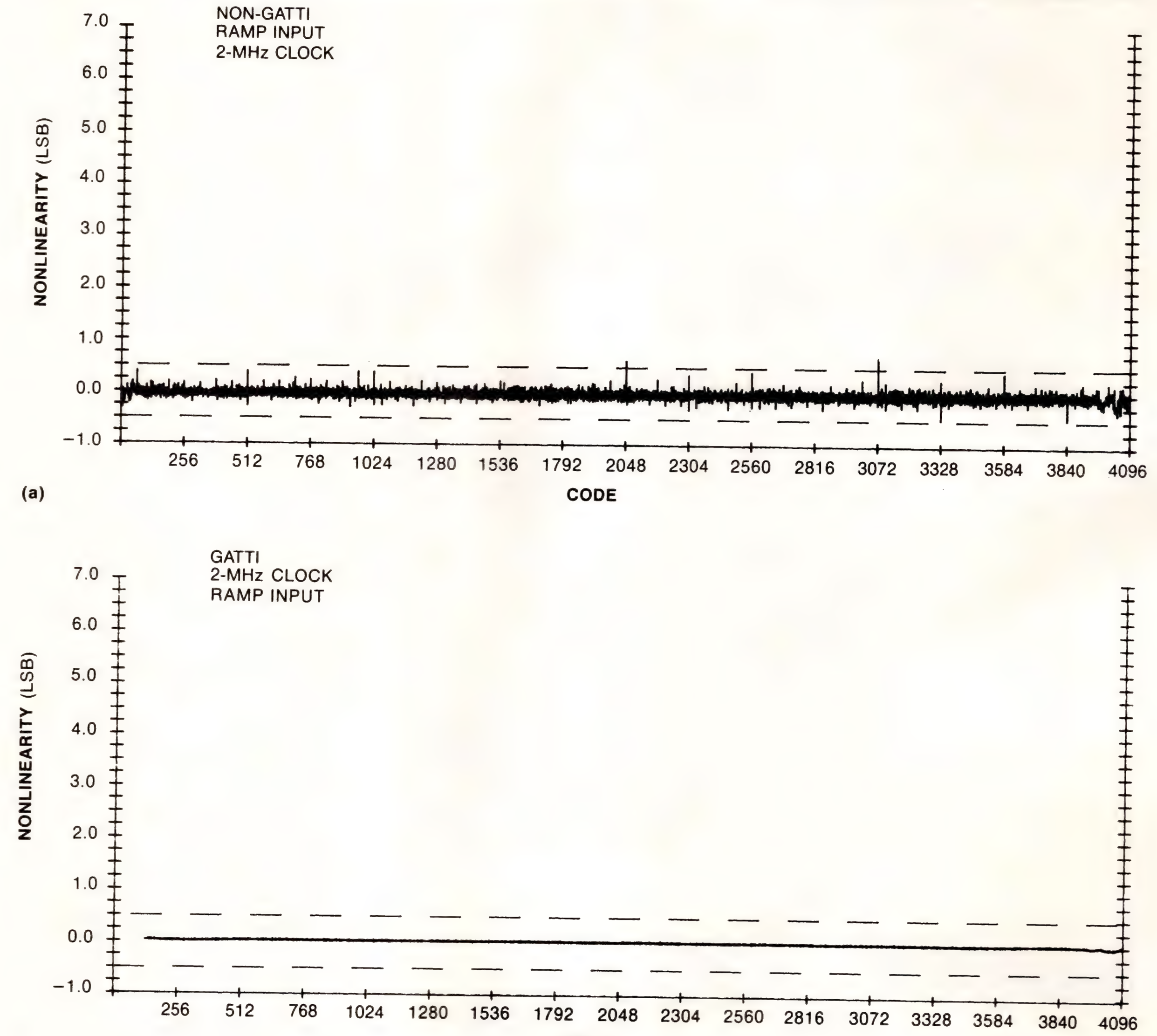

***Fig 11—Differential-nonlinearity plots for a 6.25-μsec conversion time** show that the Gatti sliding-scale technique **(b)** substantially improves the DNL of an Am6112 12-bit A/D converter.*

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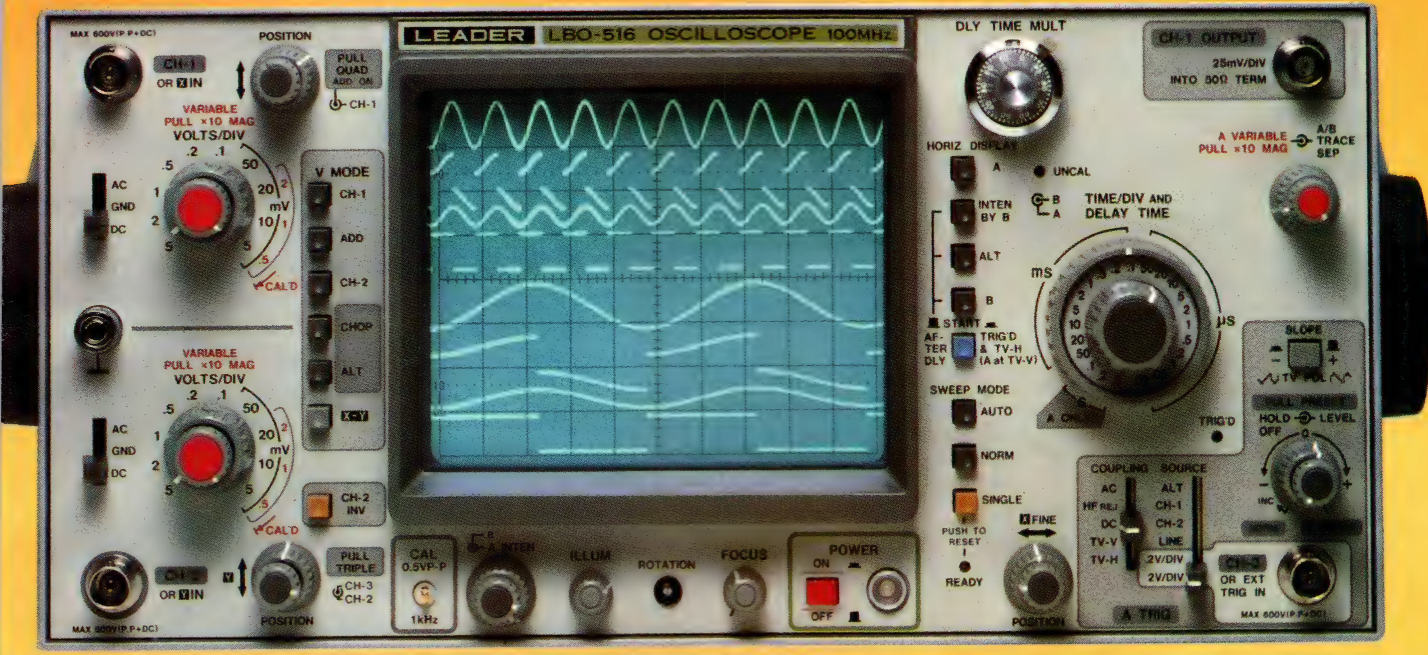

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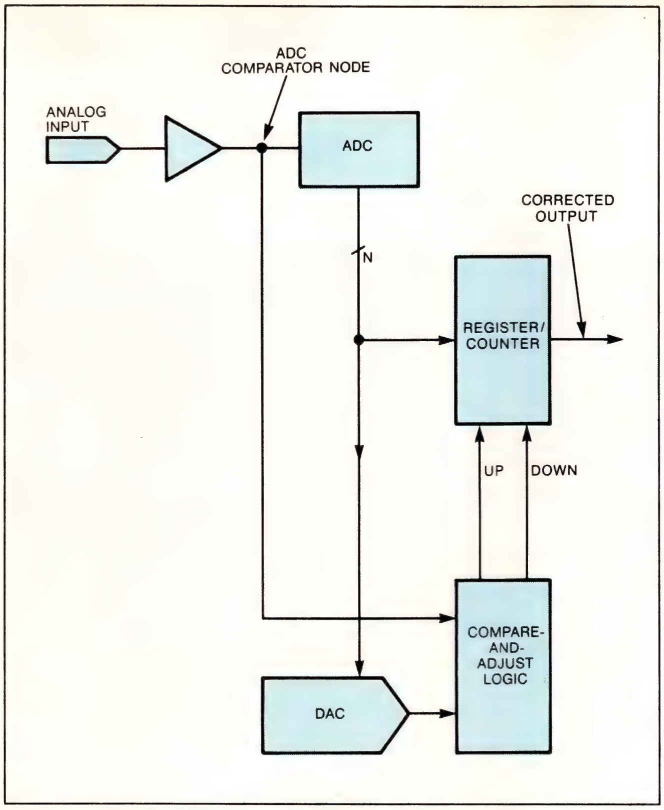

Fig 12—Error correction absolves all sins *in a successive-approximation A/D converter. The technique allows you to clock the ADC so fast that incorrect bit choices can occur early in the conversion process. The error-correction method then corrects these choices later.*

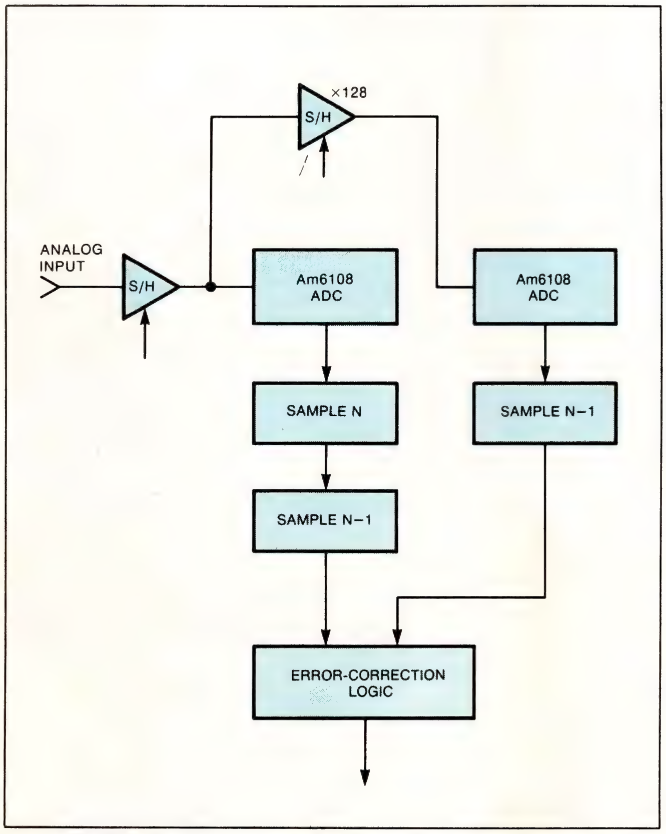

Fig 13—Using a coarse and a fine conversion cycle, *this pipelined approach to error correction allows you to clock a successive-approximation A/D converter at much higher rates than an uncorrected ADC could accommodate.*

passes of the input ramp. This result shows a slight improvement over that of **Fig 9a** because the effect of the random comparator uncertainty is reduced by averaging. **Fig 9d** shows the effect of applying the Gatti method for 10 passes of the input ramp. Notice the significant reduction in DNL variation.

In **Fig 10,** the Am6112 test board used in the original differential-nonlinearity tests is modified to incorporate the offset DAC, a 7-bit pseudorandom binary shift register for offset selection, and three 4-bit adder chips to subtract the digital value of the offset from the ADC's output. The results, shown in the DNL plots of **Fig 11a** and **11b,** show that the Gatti method reduces DNL to about 6% of a code width.

Error-correction hardware methods for A/D converters are of particular interest because they hold out the possibility not only of reducing differential nonlinearity but also of improving the absolute accuracy of the ADC while reducing conversion time. Progressive clocking permits faster operation before errors occur, whereas the Gatti method enhances bit-width uniformity at the expense of single-shot accuracy.

Error correction allows you to clock the converter so fast that incorrect bit choices occur early in the conversion cycle. The idea here is to compare the residual voltage at the comparator's input with the actual analog input at an appropriate place in the normal successive-approximation conversion cycle and to use this difference to correct the digital output up or down by one or two LSBs before resuming the normal successive-approximation conversion cycle **(Fig 12).**

The correction typically takes place either at the eighth bit (for 12-bit converters) or at the end of the conversion cycle. Insertion of the correction cycle has two effects: It reduces settling-time requirements for the input sample/hold amplifier, and it allows you to run the ADC so fast that wrong bit decisions occur early in the conversion cycle (and are corrected for later). If the correction occurs at the end of a conversion, then you can use two ADCs to pipeline the total conversion by using a coarse and a fine conversion cycle **(Fig 13).**

While the first ADC performs a coarse 12-bit conversion, the second ADC converts an amplified version (from a second sample/hold amplifier) of the first ADC's previous residual comparator-node voltage. The error-correction logic uses the output of the second ADC to adjust the output of the first ADC, thus achieving a correct result. (For a description of a nonpipelined variation of this technique, consult **Ref 2.**) You can use error correction in conjunction with both the progres-

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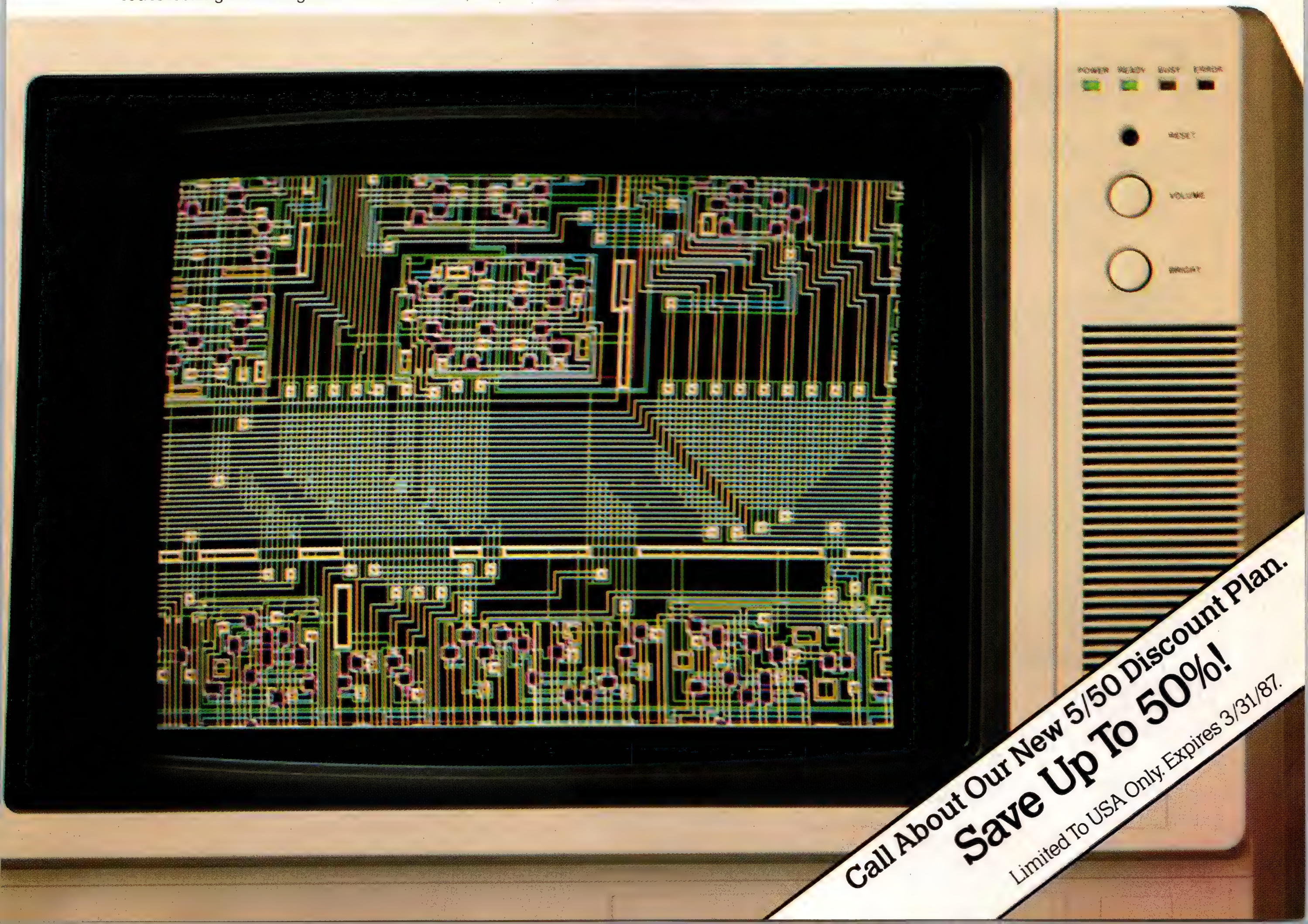

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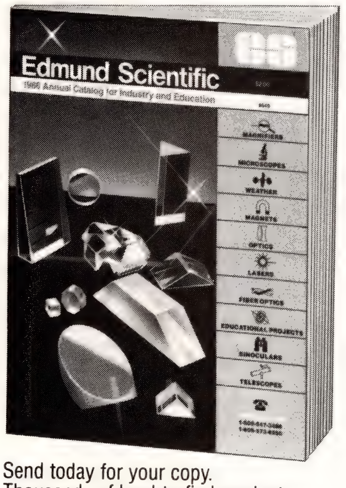

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Acknowledgment

The authors wish to acknowledge the contributions of N Adams and J Kuklewicz in devising the original Am6112 evaluation circuit and in writing the data-reduction software. They also wish to thank Dr H Speiler of UC-Lawrence Berkeley Laboratory, professor Michael Maier of Michigan State University Cyclotron Laboratory, and Dr K D Muller of the KFA, Julich (West Germany) for their valuable insights on A/D operation.

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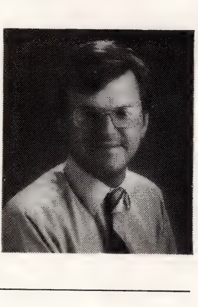

Steven Harris is a section manager in product planning at Advanced Micro Devices. Prior to joining AMD, he worked at Cooke Associates Ltd in the UK. Steven holds BSc and PhD degrees from Sussex University and is a member of the IEEE, IEE, and SID. He enjoys playing and listening to music in his leisure time.

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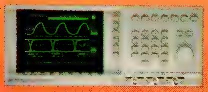

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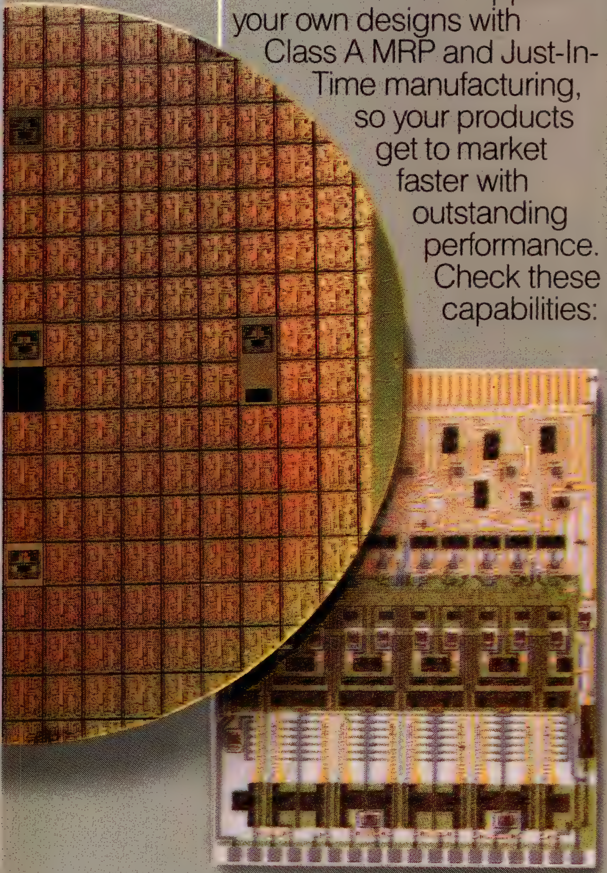

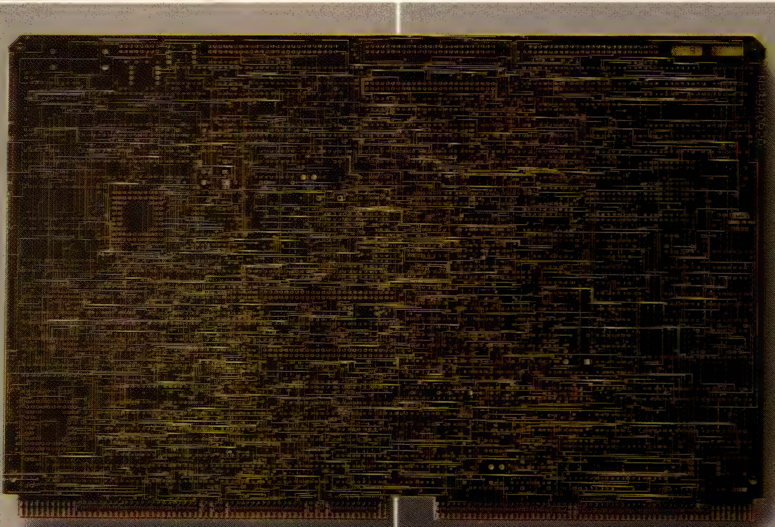

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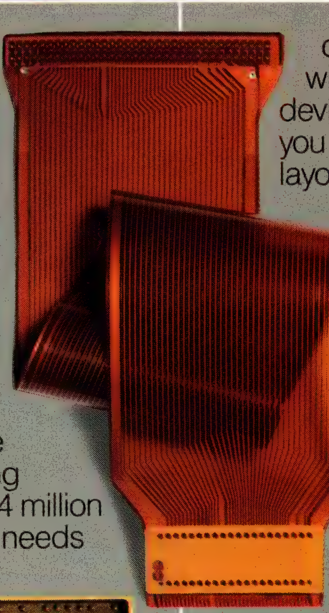

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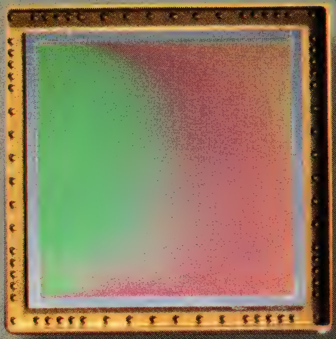

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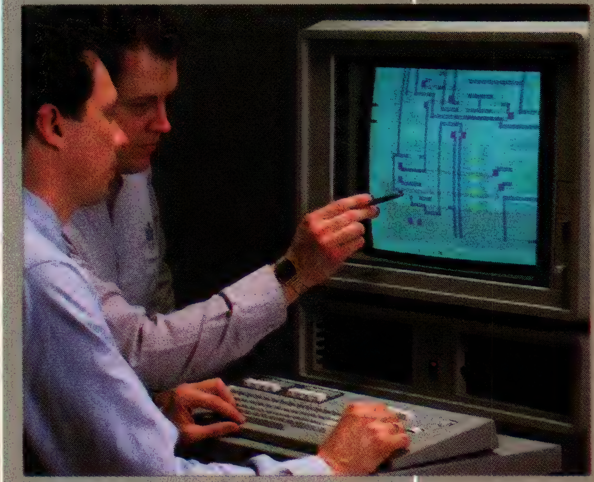

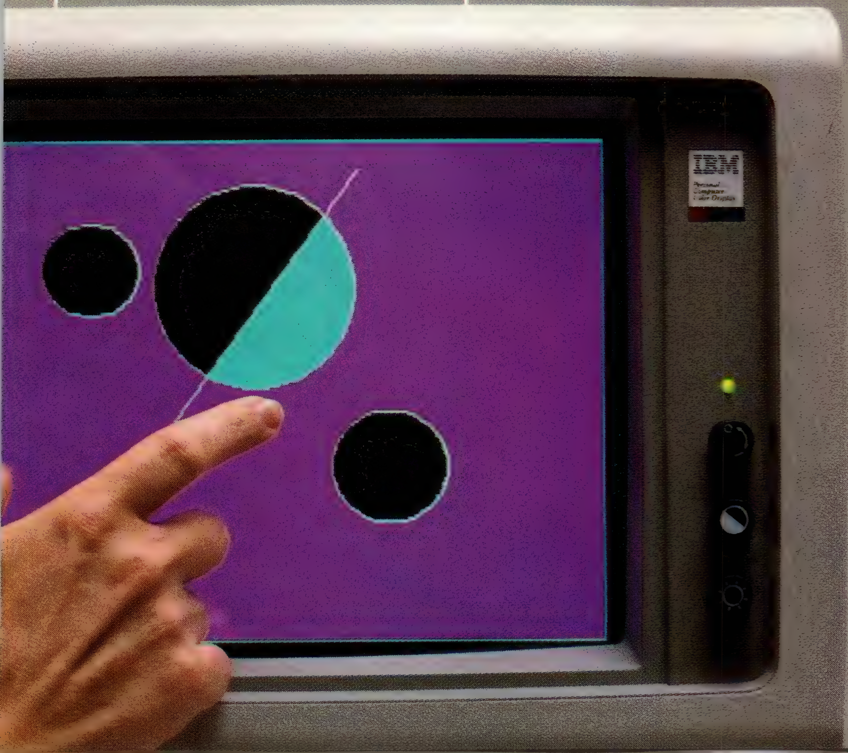

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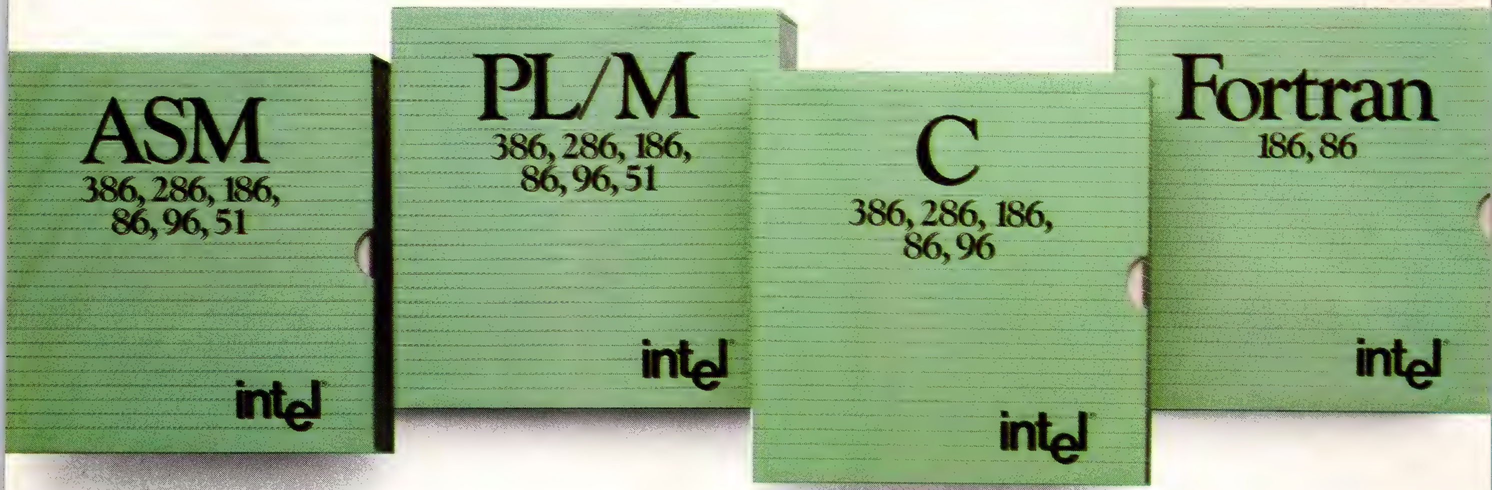

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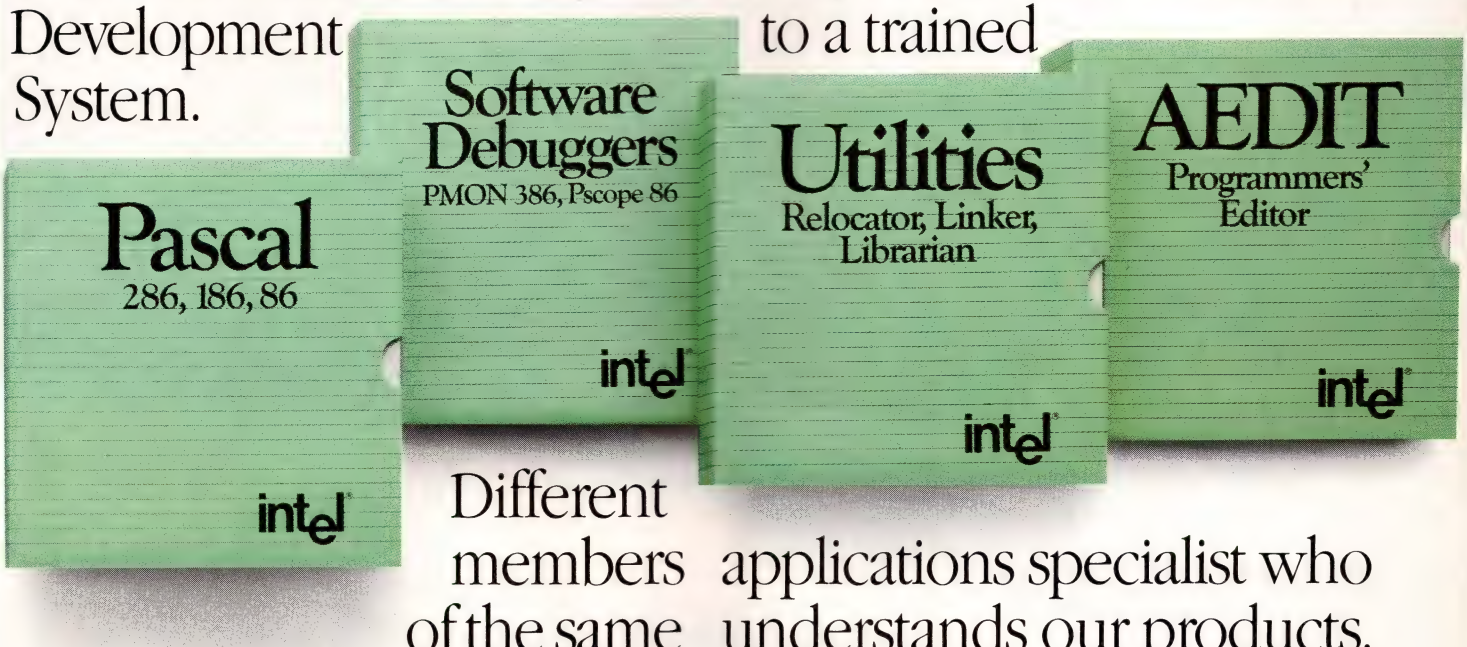

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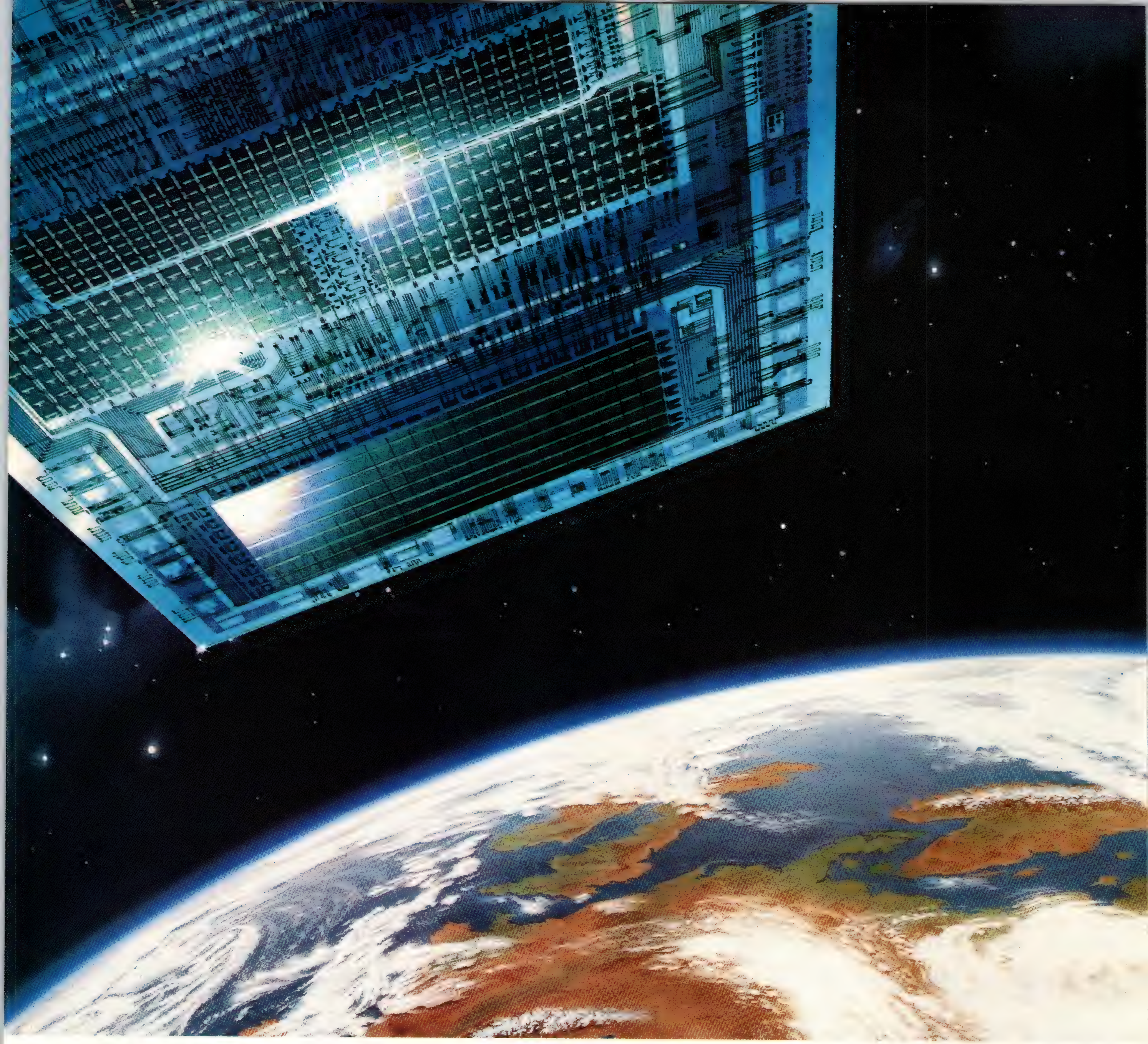

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CIRCLE NO 52

Knowing error sources lets you evaluate hard-disk drives

Because they are electromechanical parts, hard-disk drives inherently exhibit a higher failure rate than do solid-state electronic components. Understanding the sources of error in high-capacity hard-disk drives can help you institute a comprehensive program of quality assurance for your systems that use disk drives.

George Robinson, *FlexStar Corp*

With the advent of moderately priced disk-drive testers, you can now evaluate hard-disk drives before you buy them and monitor the quality of the deliveries you receive, even if you purchase drives in small volumes. In fact, you can ultimately set up an ongoing program of quality assurance for systems that use hard-disk drives.

To institute such a program, you need to test your disk drives during the various phases of system development. For instance, when you're choosing a drive, you'll want to evaluate its recording channels, measure its access time, and check for any start/stop effects or thermal off-track effects. When you're evaluating the drive for use in your system, you'll need to identify any defects in the drive, perform environmental and life testing, and measure the drive's voltage margins.

At the system-integration and production stages, you'll need to check the drives either during or after burn-in, and you'll have to perform system tests and fine-tune your system-manufacturing process. During these final tests, you'll want to create a database for ongoing reliability analysis.

Before you can create a regimen for drive evaluation and a subsequent quality-assurance program, you must understand the possible sources of error in a disk drive. The first, most critical requirement for satisfactory disk-drive performance is the accurate alignment of the read/write heads with respect to the data, under all conditions of operation. The principal causes of imperfect head alignment are thermal effects, mechanical wear, obstacles to the repeatable positioning of mechanical components, and positioning hysteresis.

Temperature changes during operation generally affect drive performance much more than do constant high or low temperatures. A manufacturer can minimize the effects of constant temperature on the mechanism by fabricating the drive with certain materials, but it's more difficult to compensate for the changing temperatures produced by self-heating during initial start-up and by system cooling methods, for example. Note that heat can also cause mechanical distortion of drive components in a drive that's improperly mounted to the system frame. Humidity normally has only secondary effects on the thermal behavior of the drive, but moisture (condensation) may accelerate corrosion and aging.

The most critical requirement for good disk-drive performance is that the read/write heads be accurately aligned with respect to the data.

The effects of mechanical wear usually won't appear during short-term testing, but be sure to watch for accelerated abrasion, which can be caused by improper manufacture or assembly of the drive's mechanical components. Minor mechanical defects in stepping motors and sensors can result in slight shifts in the symmetry of the head positioning over odd- and even-numbered tracks. This displacement is likely to be constant over a wide range of tracks, however.

Sources of head-positioning error

The ability of the head-positioning mechanism to return to precisely the same place at the end of each seek operation is crucial to reliable data recovery. Factors that can impair this ability include friction, asymmetry in the operation of motors, and positioning hysteresis (**Fig 1**).

Hysteresis is an electromechanical phenomenon in which the drive head comes to rest at a different position after a forward seek than after a reverse seek. The effect is usually very small in high-gain servo-positioning mechanisms, but it may be important in open-loop positioning systems. Many drives that use stepper motors for head positioning avoid this problem by overstepping on a reverse seek so that the last step to the desired track is always in the forward direction.

When you're testing a drive's head-positioning mechanism, you should avoid simple seeking patterns. For example, seek operations to all odd-numbered tracks in the forward direction, and all even-numbered tracks in the reverse direction, may not reveal deficiencies caused by motor asymmetry or positioning hysteresis. You'll need a more complex pattern—one that approaches randomness—to uncover such defects.

Further, when you're performing temperature testing, you'll have to consider the effect of the temperature conditions under which the data was recorded. You may find that the error rates you obtain correlate with the difference between the temperature at which data was recorded and the temperature at which it was read back. To achieve the complex seek patterns needed to reveal the more subtle deficiencies of a drive, you'll need a programmable tester with plenty of storage in which to set up the test patterns and analyze the results.

Data-error rates are the measure of quality

The electrical properties of a drive's read/write channel have a very large influence on error rates. One difficulty that you may encounter is that modern disk-drive electronics tolerate a greater degree of error than do those in older devices, even though they also require more accuracy than older devices did. Further, the newer disk drives have no guard band between data tracks, and their signal-to-noise ratio deteriorates rapidly as head-positioning errors increase (**Fig 2**). However, the read/write channel may be sensitive enough and have sufficient signal-regeneration capability to mask quite large head-positioning errors, so it's often harder for you to observe errors in these modern drives.

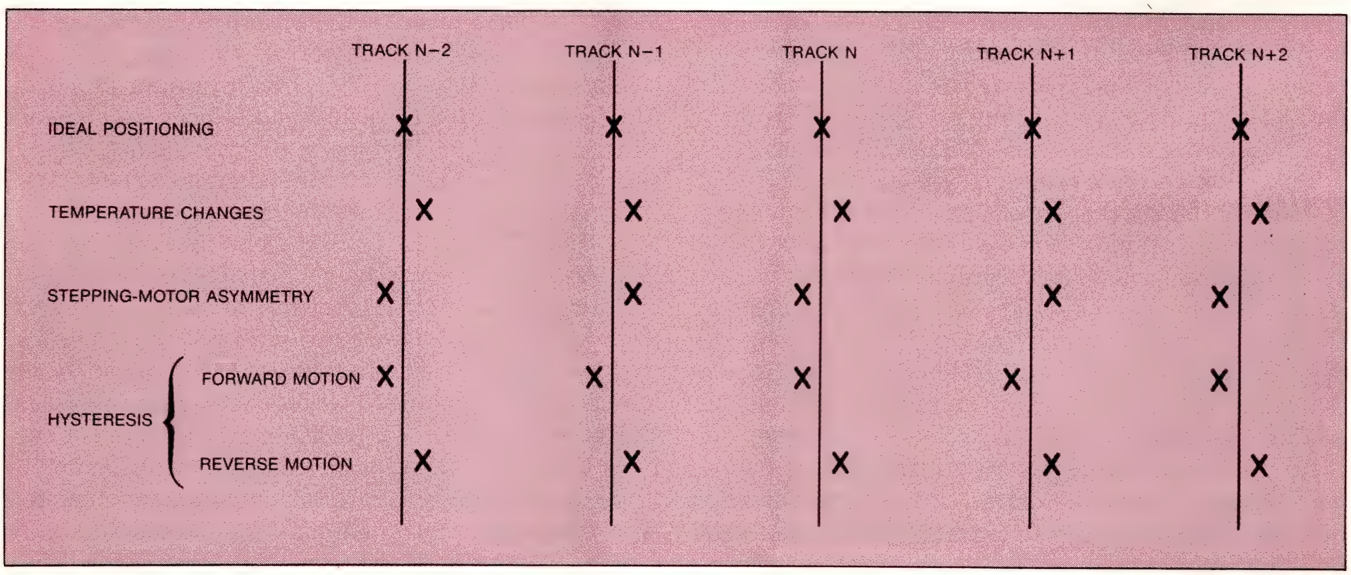


Fig 1—Incorrect head position after a seek *is the enemy of reliable data in a disk drive. Some defects cause a head-position error that's constant over the whole data area. Other defects cause more subtle positioning errors.*

Timing distortions in the drive's playback signal serve as a measure of the quality of a recording channel. You can determine the channel's quality by measuring its bit shift and resolution. Phase margin is the channel's tolerance for electrical error. (To find the tolerance for electrical error, you subtract all mechanical error from the drive's total error tolerance.) The greater the phase margin, the better the channel.

Defects in the magnetic medium can cause error

Even in channels that have wide margins, and thus great tolerance for abnormal conditions, minute defects in the magnetic medium can cause errors that are restricted to a very small physical area on the drive. Such defects may be the result of manufacturing imperfections, or of damage during operation. The channel's tolerance of defects of this kind depends on the phase margin as well as on the severity of the defects.

If the disk drive under test has any such defects, you'll observe regularly repeated errors, from which no recovery is possible, at the same physical position on the drive, as defined by the head (surface), cylinder (radial position on that surface), and byte displacement (angular location from the index reference). Hard errors of this kind are easier to deal with than are the intermittent soft errors that characterize marginal defect conditions: In drives that exhibit hard errors, you can isolate the bad tracks, preventing any use of them.

To test a read/write channel thoroughly, you'll require a tester that has a very stable clock. The tester should allow you to measure margins and data timings with a repeatability of 2 nsec or less. You'll have to be able to control the width of the playback timing window in order to find marginal error locations. Further, your tester should be able to measure margins, and it should be capable of narrowing the timing window to accelerate the occurrence of errors. Narrowing the timing window not only pinpoints defects in the magnetic medium, but also reveals read/write channels that have insufficient reserve margin to compensate for the effects of temperature **(Fig 3)**.

Unlike a tape or floppy-disk drive, in which the read/write head actually touches the disk medium, thus gradually degrading the quality of the recorded data, a hard-disk drive does not degrade the data stored on it. In a hard-disk drive, the heads fly over a thin film of air that separates them from the disk surfaces. Because the heads don't abrade the medium, data life on hard disks is theoretically unlimited.

In practice, however, data stored on a rigid disk is vulnerable to contact wear during the start-up and shutdown periods, as well as to the effects of particulate contamination during normal operation. Even tiny particles whose diameter is far smaller than that of a human hair are much larger than the gap between the head and the disk. When the disk is turning at full

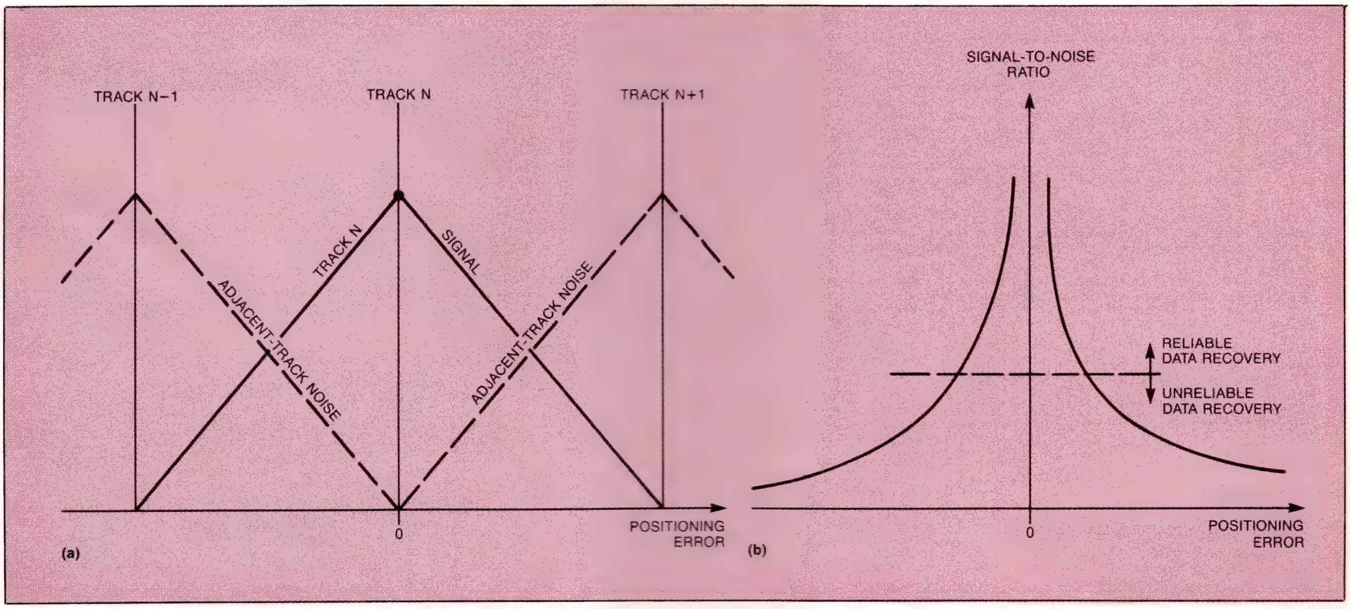


Fig 2—A misaligned head can pick up data from an adjacent track *as well as from the desired track* ***(a)****. Data errors occur when the adjacent-track signal is strong enough to be detected by the read/write channel. A poor signal/noise ratio in the read/write channel* ***(b)*** *can also cause data errors.*

Factors that may impair the reliability of head-positioning mechanisms include friction, motor asymmetry, and hysteresis.

speed, a particle carried in the air stream can cause the head to bounce sharply and touch the disk surface. The impact can score or pit the surface, causing loss of data or, in extreme cases, permanent damage to the head, the disk surface, or both.

Another potential problem is accentuated by drive manufacturers' continuing efforts to develop smaller, lower-power drives. The small, brushless dc spindle motors in 5¼-in. and smaller hard-disk drives are sometimes unable to accelerate the disks reliably to full rotational speed. To operate correctly, the motor must generate a torque that is adequate to overcome the mechanical stiction (static friction) of the disk at rest, as well as the friction between the heads and the disk surfaces. The drag of the heads before they reach flying speed, together with variations in spindle-motor torque, can lead to marginal operation that becomes worse with age. Also, if the heads are not parked outside the data area, they can abrade the disk, causing degradation or loss of data.

Practical tests and equipment calibration

Measurement of phase margins, which has become the standard method of characterizing MFM (modified frequency modulation) disk subsystems, has some value in testing machines that use the newer run-length-limited (RLL) encoding methods. To test MFM and RLL channels, you set the clock frequency so that one clock period is equal to one bit-time at the specified data rate; the window during which reading takes place is normally the full width of a bit cell (or clock pulse), but you progressively reduce the width of this window until data errors start to appear. The amount of reduction that you achieve before errors appear represents the timing safety band, or phase margin. The most reliable channels have the largest phase margins.

The drive components that contribute most to margin loss are the head/disk assembly, the read/write channel electronics, and the data-separation circuits. Data separation consists of dividing a single bit stream containing both clock and data pulses into two separate streams, one containing clock pulses only and the other containing data pulses only. In drives that have an ST-506 interface to the host, data separation takes place in the disk-drive controller; thus, you can measure phase margins at the interface. However, you must be careful that your test results reflect only the characteristics of the drive under test and not any contribution from the data separator.

Thermal cycling is an effective way of inducing extremes of head mispositioning. This technique reveals defects that you wouldn't find if you merely were to record all tracks at the same temperature and then read them back. You can obtain worst-case data on the

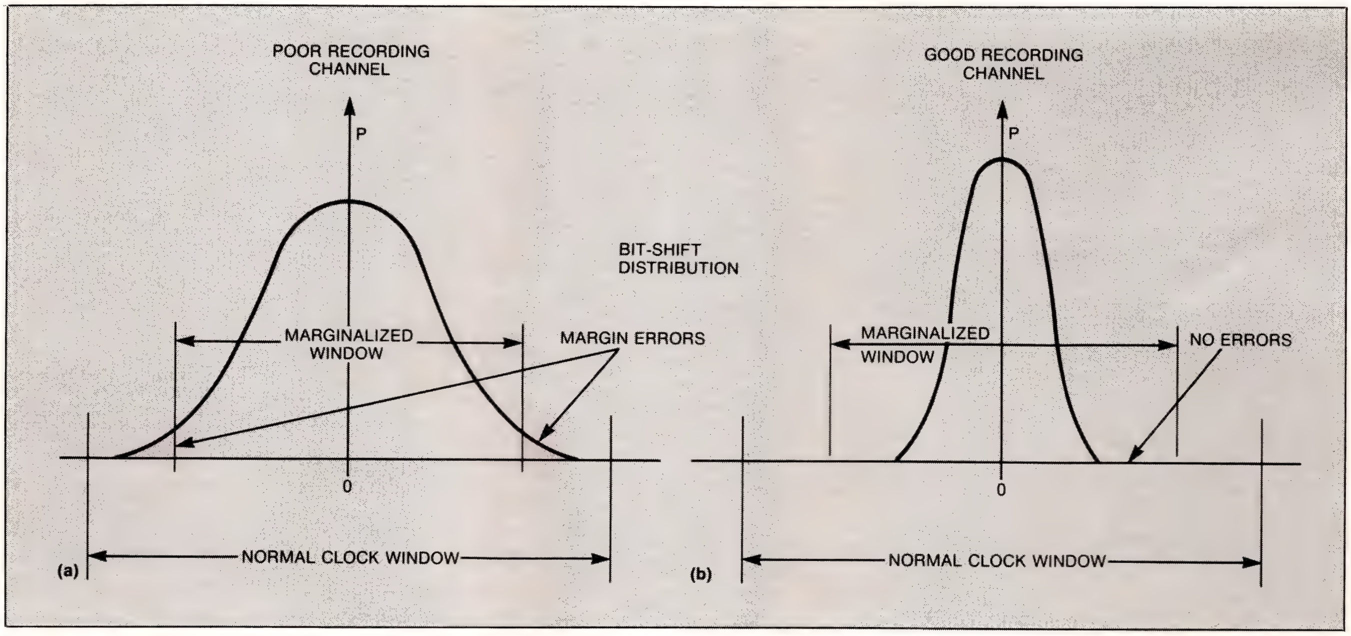


Fig 3—Margin errors occur *when you can't shift the center point of the read/write response curve without inducing errors* ***(a)****. The response of a good read/write channel* ***(b)*** *is such that it can correctly read data pulses that occur before or after the nominal center point of the reading window.*

Testers outsmart smart disk drives

To test disk drives using interfaces other than the common ST-506/412 drive interface, you'll need special drive testers. ESDI (Enhanced Small Disk Interface) drives, for instance, have a higher data rate than do ST-506/412 drives. Because of their higher data rates, ESDI drives require much tighter control of timing windows and margin circuits, and, in turn, they require that the data-clocking circuits be located on the disk drive. To test ESDI drives, therefore, you'll need special test points within the disk drive. You can use the FlexStar FS8600 ESDI tester to evaluate these drives.

You'll also need special testers for drives having intelligent interfaces such as SCSI (Small Computer System Interface) and IPI (Intelligent Peripheral Interface). Unlike the relatively primitive ST-506/412 and ESDI drives, which require the controller circuitry or the host computer to provide disk-support activities such as address calculation, error retry and correction, and data clocking, intelligent disk-drive interfaces such as SCSI and IPI conceal the details of device operation from the system.

These intelligent interfaces allow the host computer to issue high-level commands such as Format, Seek, Read, or Write, which are universal in character. The device electronics interpret these commands and generate the device-level signals needed to execute them. **Fig A** summarizes the differences between device-level and intelligent interfaces from a product-testing point of view.

To test intelligent drives, therefore, you need a disk-drive tester that can bypass the system interface. You can test SCSI drives, for example, by using an instrument like the FlexStar FS6000 SCSI tester, which lets you perform both data-margin testing and analog-dropout analysis with the aid of a special analog probe. The tester also lets you circumvent the intelligent interface to perform disk-defect identification in factory settings.

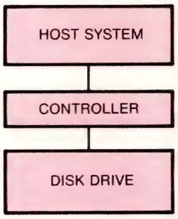
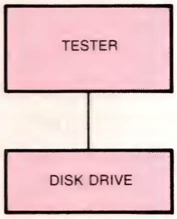
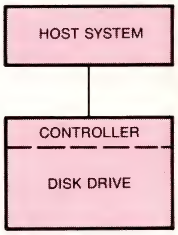
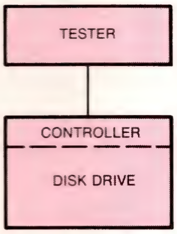
TYPE	APPLICATION CONFIGURATION	TEST CONFIGURATION	ADVANTAGES	DISADVANTAGES
DEVICE-LEVEL INTERFACE (ST-506)			TESTER SIMPLICITY WIDE ACCEPTANCE MARGINALIZED DATA HANDLING	DEFECT-MAP HANDLING ERROR-RECOVERY PROCEDURES ARE IN HOST
INTELLIGENT INTERFACE (SCSI)			ERROR-RECOVERY PROCEDURES IN DRIVE DEFECTS RETIRED DURING MANUFACTURE TRANSPARENT ERROR CORRECTION	DRIVE QUALITY CAN'T BE TESTED THROUGH INTERFACE DEFECT MAPPING REQUIRES TEST PORT COMPLEX TESTER

***Fig A—Device-level interfaces are sparing of hardware** and allow great flexibility in testing procedures. Intelligent interfaces simplify the system designer's task but make the task of the product tester more complex.*

Temperature changes have more effect on error rates than do steady-state thermal conditions.

mechanical intrusion of adjacent tracks by recording all the tracks at room temperature and then rerecording alternate tracks at extremes of temperature. You can then determine the worst-case results of temperature changes by comparing the tracks recorded at extreme temperatures with those recorded at normal room temperature.

To evaluate the complex effects of temperature on a drive's performance, you'll need a good temperature chamber with a range that extends at least 3°C beyond the minimum and maximum operating temperatures specified by the drive manufacturer. It isn't essential for you to have control over the rate of temperature change, but such control will facilitate testing if the system using the drive will be subject to large or rapid temperature changes.

Further, although most disk drives have adequate compensation for temperature effects under steady-state conditions, the differing thermal masses of the drives' mechanical components and support structures can create critical misregistration and misalignment during temperature transitions. You can hasten the testing process by using test patterns that examine only narrow portions of the inner and outer zones of the recording area.

If life tests are important for your application, you'll need to program your tester to check for any signal degradation caused by disk-surface abrasion by the heads during 10,000 start/stop cycles. You can use the same life test to determine whether any breakdown of head/disk lubrication or any buildup of starting friction is impairing the ability of the drive to start reliably. Another way of establishing the degree of mechanical wear is to sample particle counts within the sealed disk chamber at regular intervals during start/stop life tests.

Although testing equipment at voltage margins is good practice, it's generally too costly (you need expensive programmable power supplies) and time-consuming to be of benefit to small-volume users. In fact, although it generally pays to check drive manufacturers' specs, you don't need to perform your own voltage-margin testing, because disk-drive manufacturers do a good job of minimizing voltage-margin problems.

What's more, environmental testing is a far more powerful tool than voltage-margin testing. For example, storing the drive for an extended period in the manufacturer's container at high temperatures can reveal the potential deterioration of seals and plastic parts. Bearings and other interacting parts may lose lubrication by evaporation and consequently reduce equipment life. In some cases, lubricants may seep to places where they shouldn't be, causing early failure of the equipment.

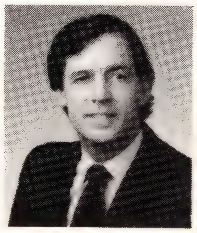
Test drives in your system

The best way to test a disk drive's power requirements and packaging is to install the drive in the target system. The most severe power demands occur at turn-on, so you can establish the system's power requirements by measuring starting-current characteristics.

High-performance actuators need large amounts of power, and you need to take them into account when you're establishing power-supply specifications. To avoid unpleasant surprises, you should measure the system's power consumption at the limits of permissible temperatures and voltages. If your system will use two half-height drives stacked together, you should retest them in that configuration to identify any self-heating problems.

Installing a drive in the target-system's enclosure can reveal potential problems at the installation and maintenance levels, as well as at the performance level. You should check to see whether there is adequate clearance between the drive and the enclosure to accommodate the connectors, whether indicator lamps are visible, and whether a technician will be able to see and set configuration switches when the drives are installed. **EDN**

Author's biography



George Robinson, president of FlexStar Corp (Milpitas, CA), has many years of experience in the design, manufacture, and testing of disk drives. George attended Kent State University, and he worked for Shugart Associates before starting FlexStar. In his spare time he enjoys tennis and basketball.

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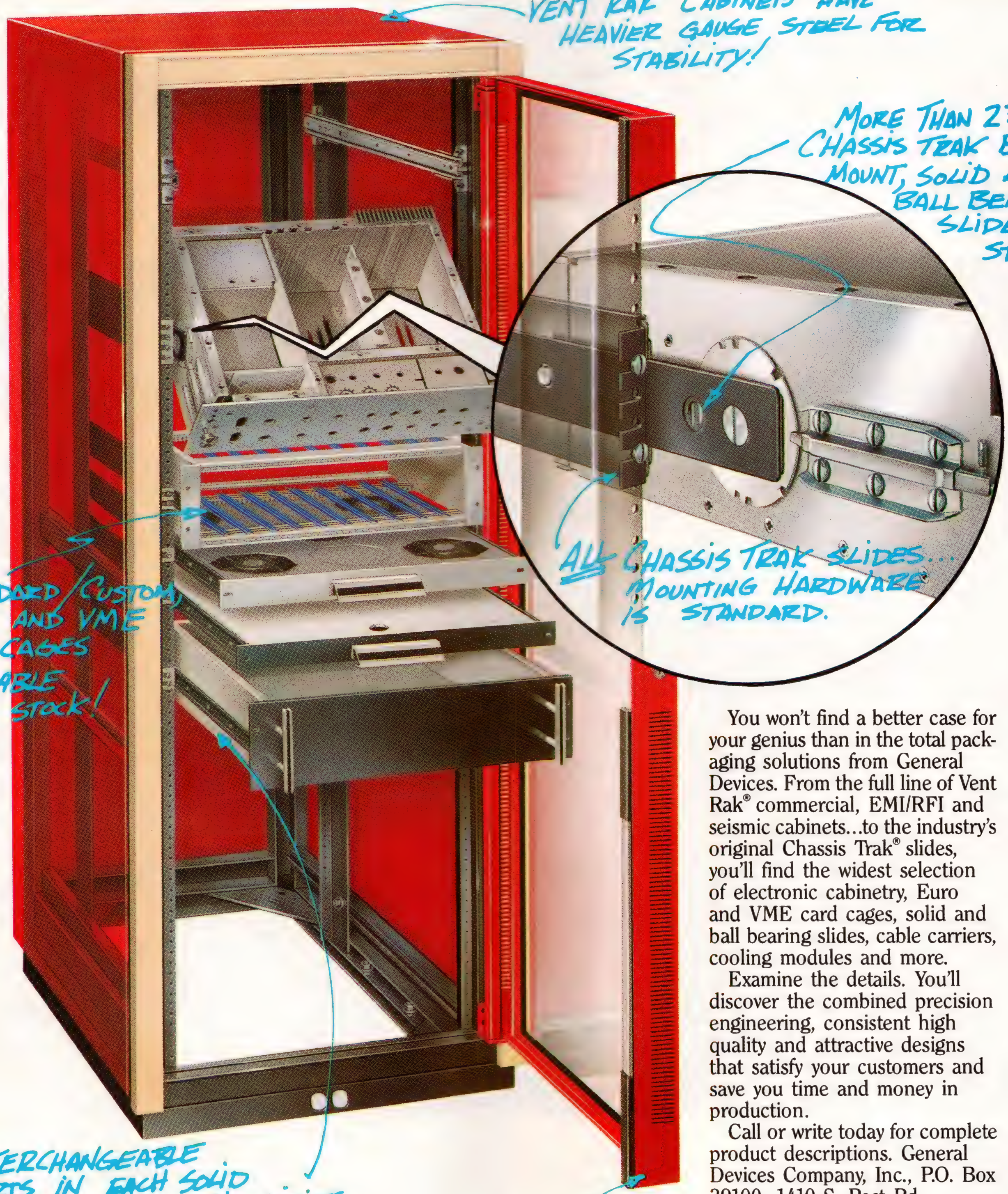

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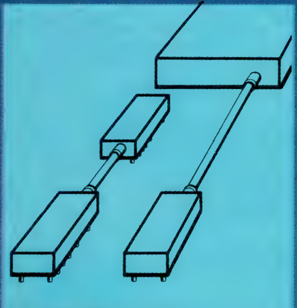
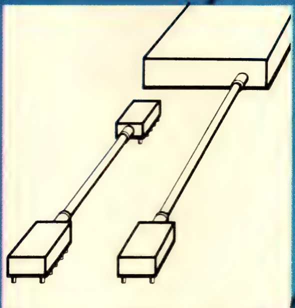
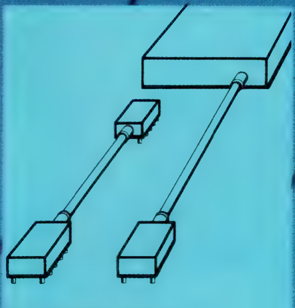


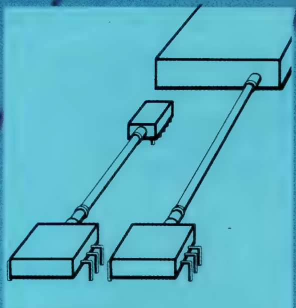
Transmission system for 0 to 10 MBd
Range with LED: about 4 km
Range with laser: about 40 km



Transmission system for 5 to 50 MBd
Range with LED: about 2 km
Range with laser: about 20 km*
* under development



Transmission system for 10 to 130 MBd
Range with LED: about 4 km
Range with laser: about 30 km



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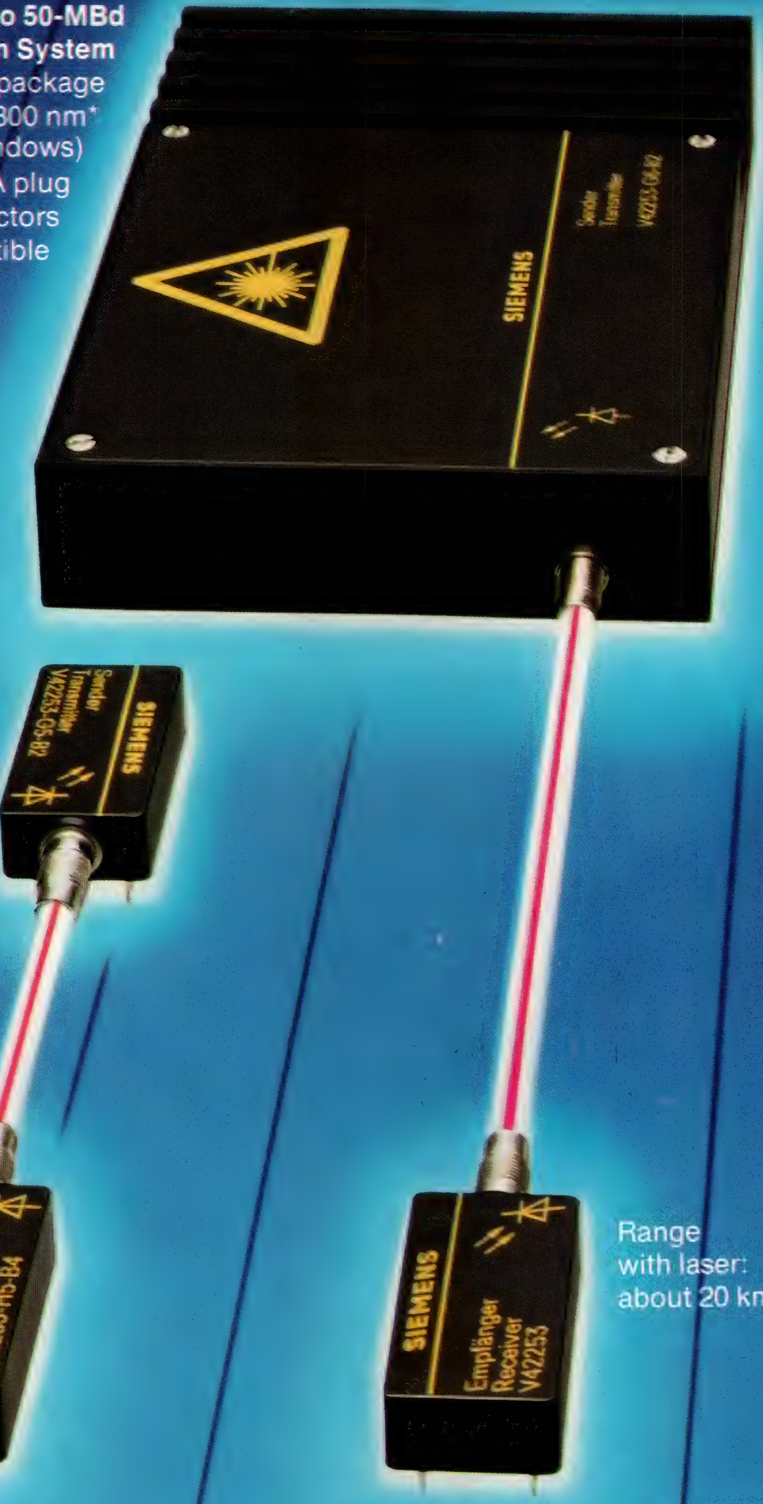
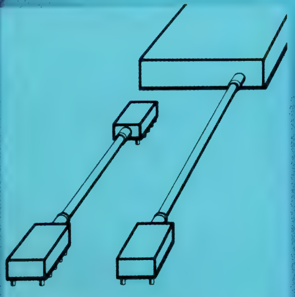


Range
with LED:
about 2 km

Range
with laser:
about 20 km



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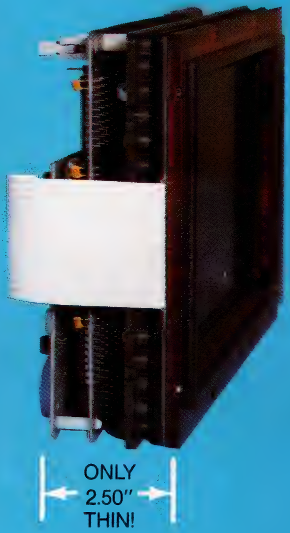

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CIRCLE NO 56

Designer's Guide to EDIF—Part 2

Use an interchange format to port component libraries

This article, the second of a 4-part series, shows you how to translate your semicustom libraries into the Electronic Design Interchange Format so that you can transfer the libraries to any CAE system or ASIC foundry that accepts this format. You can use EDIF to create schematic, behavioral, and physical representations of the components.

Mike Waters, Esther Marx, and Hart Switzer,
Motorola Inc

If your CAE system can't access every component library that you need, you may be better off without that CAE system. Unfortunately, every ASIC or standard-component vendor maintains its library in its own format, so no matter what CAE system you have, it probably can't read every available component library. The Electronic Design Interchange Format (EDIF) eliminates the problem of transferring library files. In this installment of a 4-part series on EDIF, you'll learn how to render the schematic, behavioral, and physical aspects of your component library in EDIF.

EDIF is a public-domain format for the presentation and ordering of schematics, symbolic and physical layouts, digital and analog designs, interconnections, and text. The specification lets any CAE system communicate with any ASIC or standard-component library. By using EDIF, then, any ASIC vendor can transfer accurate and complete semicustom-IC libraries to any user. As a designer, you can also transfer libraries between incompatible CAE/CAD systems. EDIF can describe semicustom ICs, custom ICs, standard ICs, passive components, board-level parts, or complete modules.

If you are a CAE-system user, you don't need to know EDIF to use it. EDIF-interface software can handle all EDIF operations. But although you can use EDIF without learning all the keywords, you should learn the overall structure of the format in order to set

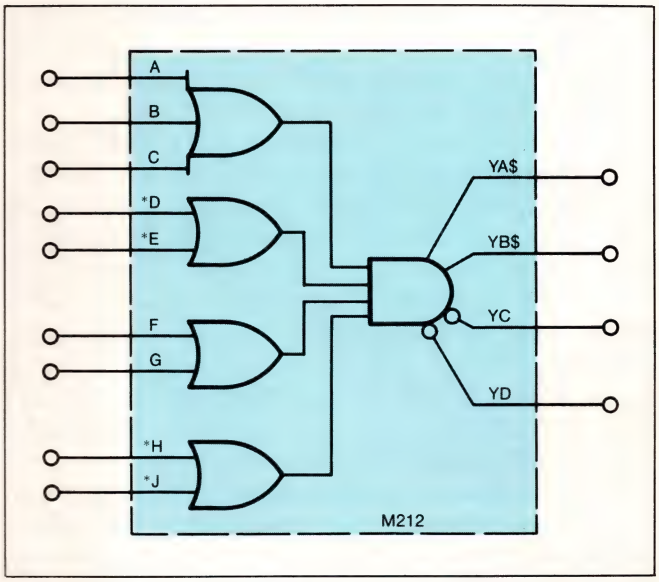

Fig 1—Using the EDIF file *given in* ***Listing 1,*** *a workstation will generate this symbol for the M212 bipolar 3-2-2-2 OR/AND macrocell.*

Although you can use EDIF without learning all the keywords, you must learn the overall structure of the format if it's up to you to build the files for translation.

up the EDIF files for transfer. (If you want to learn all the details of EDIF, or obtain copies of the EDIF specification, contact the EDIF User Group, 2222 S Dobson Rd, Bldg 5, Mesa, AZ 85202.)

Even without learning all the details of EDIF, you can appreciate the benefits of a standard data format. Such a format would enable a manufacturer of electronic components to supply a library of its products to a diverse set of CAE systems. Instead of maintaining a separate library for each CAE system, the manufacturer needs to maintain just one library.

Because the ASIC vendor would maintain only one library, the format would reduce the likelihood of errors in the library. CAE-system vendors, rather than the ASIC manufacturers, usually maintain the libraries that run on their CAE systems, and these vendors often introduce errors in an ASIC library. What's more, these libraries can contain data that is several months old. EDIF cuts down on library errors because it lets an ASIC vendor maintain its own library. After all, a manufacturer knows more about its components than anyone else, so it is in the best position to evaluate the effect of fabrication changes or design revisions. In addition, users will catch and fix errors more quickly if they share the same library.

Verify the accuracy of your components

When you use an EDIF component library, you must make certain that your library is current. You can verify the data in your library by checking the file's "accounting" field. The accounting field provides the date and version number of your data. Each revision of a master library contains a new version code.

You revise or create components in an EDIF library by isolating the appropriate portion of your file. The tree-like structure of EDIF makes it easy to isolate any part of a file. The structure that describes components in an EDIF file consists of a "library," "cells," and "views." To describe a cell in a library, you will typically use as many as four distinct view types: schematic, behavior, net-list, and symbolic (see part 1 of this series, EDN, January 22, page 153). You may also use more than one view of the same type—for example, for military and commercial versions of your design.

The schematic view describes schematic symbols. The behavior view provides models of logic-simulator primitives. The net-list view lists interconnections between schematic symbols or simulator primitives. The symbolic view specifies the rules for the physical design of the chip.

You use the schematic view to create schematic symbols. This view's graphics code can translate symbols to any workstation that accepts EDIF. A typical schematic-view file appears in **Listing 1** (listings begin on page 179). This file describes **Fig 1's** M212 bipolar 3-2-2-2 OR/AND macrocell.

The schematic view provides more than just graphics. You can assign a name and a function to each macrocell. Within each macrocell, each port can have property values. These property values define such characteristics as load factors and port names. **Listing 1** specifies the function of several pins in the OR/AND macrocell.

Each view contains an interface section and, where applicable, a contents section. In the schematic view, the interface section defines the symbols. The "define" and "portimplementation" statements specify symbol orientation, pins, and those pins that are logically equivalent to one another. The contents section describes the internal schematic, which often is proprietary. Because vendors rarely provide internal schematics, most schematics don't have a contents section.

The "userdata" section provides information that doesn't fit in EDIF. For example, **Listing 1** includes the terms "pagesize" and "pinspacing," which don't appear in the EDIF specification. EDIF provides a framework for transferring EDIF-defined terms directly from the source code to your target code. You must, however, write the special code that interprets non-EDIF terms.

Create a graphics symbol

The "body" section specifies the shape of a symbol. Within each body section, the "figuregroups" generate the symbol. A figuregroup consists of figures that have common attributes, such as a fabrication layer or color. As **Listing 1** shows, you create a symbol by breaking the symbol into lines ("paths") and arcs ("shapes"). You then combine the paths and shapes into a figuregroup.

The "fillpattern" section specifies whether a shape is filled or unfilled. Each symbol's "border" can have one of several "borderpatterns." In **Listing 1,** the borderpattern section specifies a dashed line.

You can verify the accuracy and consistency of your symbol by plotting it. The recipient of an EDIF file can, of course, change the appearance of a symbol, but the EDIF file provides a record of how the creator of the symbol wants it to look.

To build a complete macrocell library, you need a design manual and a graphics system. You use the design manual to enter the macrocells into your graphics system database. Once you have entered your schematics, your EDIF software can translate the schematics into EDIF files.

Building your logic-simulation library

After you have generated your symbol using the schematic view, you can store the behavior of your component in your EDIF simulation library. An EDIF simulation library comprises primitive elements and parts that are groups of primitive elements. You store the primitive elements in the behavior view; you store the interconnections among the primitive elements in the net-list view.

For most applications, today's EDIF primitive elements aren't detailed enough to be useful. The logical descriptions are simple truth tables; they lack such information as setup-and-hold times. Fortunately, to get started you don't need to use the behavior view. You can simply use the net-list view to group the primitive elements in your logic simulator and form all the complex logical devices in your design. The result is a gate-level model that takes a lot of CPU time but is an accurate reference to use in building better models.

Net lists link primitive elements

Whether you use the behavior view or your own simulation primitives, you use the net-list view to link the primitive elements and form macrocells or standard logical components. Because you usually have hundreds of macrocells and only a few primitive elements, the net-list view lets you eliminate most of the work involved in transferring a simulation library.

Each port description in the net-list view includes pin-to-pin timing data. For complex timing structures, you can use hierarchical cell descriptions.

Listing 2 gives the netlist-view code for the M212 macrocell (from **Fig 1**). The file models Boolean operations, but unlike the behavior-view models, it also includes rise and fall times for each input and output. The cell, view, and status sections are the same in the net-list view as in the schematic view, but the interface section in the net-list view specifies only the external ports.

The contents section describes the inner workings of a cell. In this view, the keyword "instance" calls primitive elements from your logic simulator. The keyword "parameter" specifies rise and fall times. You use the keyword "joined" to connect the ports of a primitive cell either to cell ports or to ports within the primitive. In each joined statement, the keyword "qualify" specifies the port that you are connecting.

Once you have verified your design, you must lay out your mask. You implement your layout in the mask layout view by using the physical rules that you specified in the symbolic view. Because so many technologies can implement the same logic, the symbolic view contains the most complex structure of any EDIF library. And because it has many general-purpose functions, the EDIF physical library can meet the requirements of every processing technology.

Motorola's macrocell arrays, for example, require a 3-part physical library: a base-array library, a macrocell library, and a package library. Examples of these files appear in **Listings 3, 4,** and **5. Listing 3** details the physical layout of an MCA2500ECL base array. **Listing 4** describes the M212 macrocell. The file in **Listing 5** associates the pins in a pin-grid array with the bonding pads on the MCA2500ECL base array.

To place a macrocell in a base array, you use EDIF's "socket" and "plug" keywords. The socket is the site in the base array that accepts the macrocell. In the socket section, you define your array's placement rules, site symmetry, and site positions. The sites in a base array can be pad drivers, output drivers, or internal sites.

To save space in a macrocell array, you can group each set of four internal sites into a "quad." Each macrocell in the group of four has access to the routing channels, so you can still access all ports on every macrocell. To place each quad into the base array, you use the "instance" keyword. You complete your macrocell placement by using the "step" keyword to specify the space between each quad.

You can store your layout in a fully expanded listing or in a hierarchical database of quads. The hierarchical database cuts the size of the file by a factor of four and gives added information that can be used during cell placement.

You can store routing barriers in a hierarchical database. To define your routing barriers, you use a body section to define a protection frame. The body consists of shapes from the appropriate figuregroups. The figuregroup statement also lets you add text and logos to your layout.

In your macrocell layouts, you use plugs to complement the sockets in your base-array layout. In the macrocell definition, you can specify macrocell-related routing barriers, port names, port locations, and internal port-to-port connections.

The border in a macrocell file creates the layout

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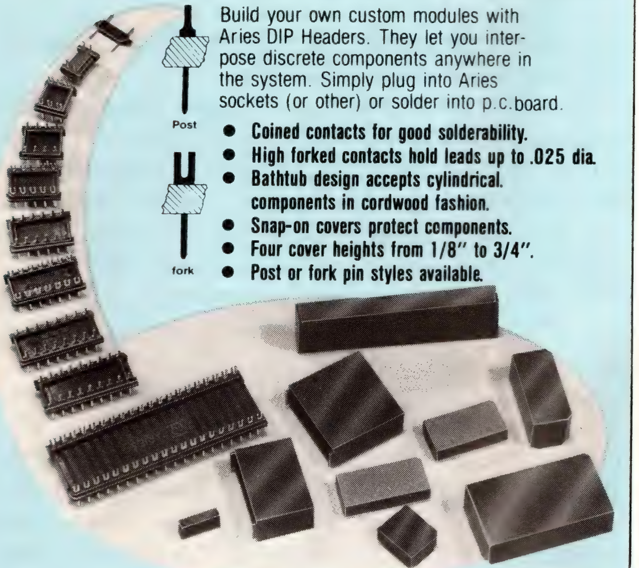

See EEM Vol. C, pgs. 1185-1190

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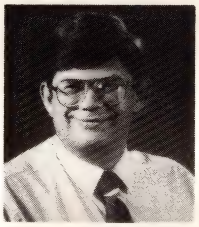
symbol. A portimplementation statement defines the location of the symbol's ports. By specifying that two ports are connected, you can pass a signal through the cell. In **Listing 4,** for example, a "joined" statement specifies that ports YD and SYD are connected in your design. You complete the description of your macrocell with the "socketset" statements, which specify cell placements and the orientation of cells in their sites.

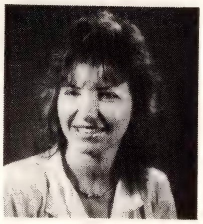
EDIF doesn't yet allow you to adjust cells to fit the available chip area or the drive requirements of a circuit. Package descriptions don't yet include the means to let you describe heat-dissipation requirements or listings of pin locations for pc-board routing.

The remaining articles in this series will show you how to create and transfer test patterns and how to develop EDIF interfaces for your own CAD operation. **EDN**

Authors' biographies



Mike Waters is a principal engineer and EDIF project manager at Motorola Semiconductor Products (Mesa, AZ). He received a BS in computer science from Regent's College in New York. Mike likes to exchange ideas with other EDN readers via his ham radio (license AA4MW) or his amateur packet radio.



Esther Marx is a senior software engineer at Motorola Semiconductor Product Sector's ASIC Division. She received an MS from George Washington University and a BA from Oberlin College. Before joining Motorola, Esther served five years in the Air Force. She enjoys writing science fiction and collecting Star Trek memorabilia.

Hart Switzer is a software engineer with Motorola Semiconductor Products, where she designs and implements EDIF software. She received a BS from Stanford University. Hart enjoys gardening and collecting antiques.

Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475

LISTING 1—SCHEMATIC VIEW OF THE M212 MACROCELL

```
(CELL M212
 (STATUS (EDIFVERSION 1 0 0)(EDIFLEVEL 0)
  (WRITTEN (TIMESTAMP 1986 6 6 16 37 42 21)(ACCOUNTING PROGRAM ''SYM2EDIF V2.00'')
   (ACCOUNTING AUTHOR ''MOTOROLA SEMI-CUSTOM'')))
 (VIEW SCHEMATIC MACRO_SCHEMATIC
  (INTERFACE
   (USERDATA PAGESIZE (POINT -125000 -125000)(POINT 125000 125000))
   (USERDATA PINSPACING 2500)(DEFINE INPUT PORT A)
   (PORTIMPLEMENTATION A (FIGUREGROUP SYMBOL_PIN (DOT (POINT 0 20000)))
    (USERDATA ATTRIBUTE
     (PROPERTY PINTYPE ''IN''
      (PROPERTY DISPLAYAT (POINT -2500 20000)(POINT -1500 20500))
      (PROPERTY JUSTIFY LOWERLEFT)))
    (USERDATA ATTRIBUTE
     (PROPERTY PINNAME ''A''
      (PROPERTY DISPLAYAT (POINT 4250 20500)(POINT 5750 22000))
      (PROPERTY JUSTIFY LOWERLEFT))))(DEFINE INPUT PORT B)
   (PORTIMPLEMENTATION B. . .)(DEFINE INPUT PORT C)
          .
          .
          .
   (BODY
    (FIGUREGROUP SCHEMATIC_SYMBOL (FILLPATTERN 1 1 ''0'')
     (PATH (POINT 5000 15000)(POINT 6750 15000))
     (PATH (POINT 5000 20000)(POINT 6750 20000))
     (PATH (POINT 5000 17500)(POINT 7500 17500))
     (SHAPE
      (ARC (POINT 6750 15750)(POINT 7500 17500)(POINT 6750 19250))). . .)
    (USERDATA BORDER MACRO_BORDER
     (FIGUREGROUP BORDER (BORDERPATTERN 6 ''001111'')
      (RECTANGLE (POINT 2500 -2500)(POINT 25000 22500))))
    (USERDATA ATTRIBUTE
     (PROPERTY COMPSIZE 2
      (PROPERTY DISPLAYAT (POINT 15000 -2000)(POINT 16500 -500))
      (PROPERTY JUSTIFY LOWERLEFT)))
    (USERDATA ATTRIBUTE
     (PROPERTY MACRONAME ''M212''
      (PROPERTY DISPLAYAT (POINT 24250 -2000)(POINT 30250 -500))
      (PROPERTY JUSTIFY LOWERRIGHT)))))))
```

LISTING 2—NET-LIST VIEW OF THE M212 MACROCELL

```
(CELL M212
 (VIEW NETLIST LOGCAP
  (STATUS (EDIFVERSION 1 0 0)(EDIFLEVEL 0)
   (WRITTEN (TIMESTAMP 1986 03 21 22 15 11)
    (ACCOUNTING DATAVERSION ''REV0000000000000000'')
    (ACCOUNTING AUTHOR ''MOTOROLA INC. – ASIC PRODUCT DIV.'')
    (ACCOUNTING PROGRAM
    ''LC2EDF VERS M0770.00.001.005 ***02/27/86***'')))
  (INTERFACE (DEFINE INPUT PORT (MULTIPLE A B C D E F G H J))
   (DEFINE OUTPUT PORT (MULTIPLE YA YB YC YD)))
  (CONTENTS
   (INSTANCE (QUALIFY LOGCAP OR)NETLIST AA
    (PARAMETER RISETIME 0 FALLTIME 0))
   (JOINED AA (QUALIFY AA OUTPUT_PORT))
   (JOINED A (QUALIFY AA INPUT_PORTS_1))
   (JOINED B (QUALIFY AA INPUT_PORTS_2))
   (JOINED C (QUALIFY AA INPUT_PORTS_3))
   (INSTANCE (QUALIFY LOGCAP OR)NETLIST CC
    (PARAMETER RISETIME 0 FALLTIME 0))
   (JOINED CC (QUALIFY CC OUTPUT_PORT))
   (JOINED F (QUALIFY CC INPUT_PORTS_1))
   (JOINED G (QUALIFY CC INPUT_PORTS_2))
   (INSTANCE (QUALIFY LOGCAP OR)NETLIST YB
    (PARAMETER RISETIME 0 FALLTIME 0))
   (JOINED YB (QUALIFY YB OUTPUT_PORT))
   (JOINED YA (QUALIFY YB INPUT_PORTS_1))
   (INSTANCE (QUALIFY LOGCAP OR)NETLIST BB
    (PARAMETER RISETIME 1 FALLTIME 1))
   (JOINED BB (QUALIFY BB OUTPUT_PORT))
   (JOINED D (QUALIFY BB INPUT_PORTS_1))
```

Listings continued on pg 180

LISTING 2—NET-LIST VIEW OF THE M212 MACROCELL

```
(JOINED E (QUALIFY BB INPUT__PORTS__2))
(INSTANCE (QUALIFY LOGCAP OR)NETLIST DD
  (PARAMETER RISETIME 1 FALLTIME 1))
(JOINED DD (QUALIFY DD OUTPUT__PORT))
(JOINED H (QUALIFY DD INPUT__PORTS__1))
(JOINED J (QUALIFY DD INPUT__PORTS__2))
(INSTANCE (QUALIFY LOGCAP NOR)NETLIST YC
  (PARAMETER RISETIME 0 FALLTIME 0))
(JOINED YC (QUALIFY YC OUTPUT__PORT))
(JOINED YA (QUALIFY YC INPUT__PORTS__1))
(INSTANCE (QUALIFY LOGCAP NOR)NETLIST YD
  (PARAMETER RISETIME 0 FALLTIME 0))
(JOINED YD (QUALIFY YD OUTPUT__PORT))
(JOINED YA (QUALIFY YD INPUT__PORTS__1))
(INSTANCE (QUALIFY LOGCAP AND)NETLIST YA
  (PARAMETER RISETIME 5 FALLTIME 5))
(JOINED YA (QUALIFY YA OUTPUT__PORT))
(JOINED AA (QUALIFY YA INPUT__PORTS__1))
(JOINED BB (QUALIFY YA INPUT__PORTS__2))
(JOINED CC (QUALIFY YA INPUT__PORTS__3))
(JOINED DD (QUALIFY YA INPUT__PORTS__4))
(DEFINE LOCAL SIGNAL (MULTIPLE DD BB CC AA)))))
```

LISTING 3—BIPOLAR BASE-ARRAY DEFINITION OF THE M212 MACROCELL

```
(CELL BIPOLAR__BASE__ARRAY
  (VIEW SYMBOLIC PHYSICAL (INTERFACE
    (DEFINE INPUT PORT (MULTIPLE P002 P003 . . .
      P122 P123 P124 ))
     (DEFINE INOUT PORT (MULTIPLE P019 . . .
      P104 P105 P106 P107 ))))
   (VIEW SYMBOLIC SITE
    (COMMENT “DIMENSIONS ARE SCALED IN MM FROM FIGURE 1”
          “OF THE DATA SHEET”)
    (INTERFACE
      (ARRAYRELATEDINFO BASEARRAY))
    (CONTENTS

      (COMMENT “DEFINE VALID MACRO SITES”)

      (INSTANCE CLOCK__GENERATOR__SITE SITE ID
        (TRANSFORM R0 (TRANSLATE 59 10)))
      (INSTANCE INTERNAL__QUAD SITE SITE ID1
        (TRANSFORM R0 (TRANSLATE (STEP 19 10 10) (STEP 17 11 10))))
      (INSTANCE OUTPUT__DRIVER__QUAD__SITE SITE ID2
        (TRANSFORM R0 (TRANSLATE (STEP 19 4 10) 10)))
      (INSTANCE OUTPUT__DRIVER__QUAD__SITE SITE ID3
        (TRANSFORM R0 (TRANSLATE (STEP 19 4 10) 89)))
      (INSTANCE OUTPUT__DRIVER__QUAD__SITE SITE ID4
        (TRANSFORM R0 (TRANSLATE (STEP 79 4 10) 10)))
      (INSTANCE OUTPUT__DRIVER__QUAD__SITE SITE ID5
        (TRANSFORM R0 (TRANSLATE (STEP 69 5 10) 89)))
      (COMMENT “ROUTING PROHIBITS WHICH ARE FIXED IN THIS ARRAY”)
      (INSTANCE ARRAY__ROUTING__BARRIERS__LEVEL__1 SITE ID6
        (TRANSFORM R0 (TRANSLATE (STEP 23 10 10) (STEP 17 11 10))))
      (INSTANCE ARRAY__ROUTING__BARRIERS__LEVEL__2 SITE ID7
        (TRANSFORM R0
          (TRANSLATE (STEP 16 10 10) (STEP 17 11 10)))))))

(CELL CLOCK__GENERATOR__SITE
  (VIEW SYMBOLIC SITE
    (INTERFACE (ARRAYRELATEDINFO ARRAYSITE (SOCKET)))))

(CELL ARRAY__ROUTING__BARRIERS__LEVEL__1
  (VIEW SYMBOLIC SITE
    (INTERFACE (BODY
      (FIGUREGROUP ROUTING__LEVEL__1
        (RECTANGLE (POINT 0 2) (POINT 0 10)))))))

(CELL ARRAY__ROUTING__BARRIERS__LEVEL__2
  (VIEW SYMBOLIC SITE
    (INTERFACE (BODY
```

Listings continued on pg 182

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CIRCLE NO 64

LISTING 3—BIPOLAR BASE-ARRAY DEFINITION OF THE M212 MACROCELL

```
          (FIGUREGROUP ROUTING_LEVEL_2
            (RECTANGLE (POINT 0 10) (POINT 0 2))
            (RECTANGLE (POINT 0 5) (POINT 3 4)))))))

(CELL INTERNAL_QUAD_SITE
  (VIEW SYMBOLIC SITE
    (INTERFACE (BODY
      (FIGUREGROUP ROUTING_LEVEL_1
        (RECTANGLE (POINT 0 0) (POINT 5 6))
        (COMMENT “ROUTING LEVEL 1 IS ENTIRELY RESERVED FOR WIRING”
               “INTERNAL TO THE MACRO CELL AND APPEARS AS A SOLID”
               “BLOCKAGE TO THE ARRAY ROUTER”))))
    (CONTENTS
      (INSTANCE INTERNAL_SITE SITE IS1 )
      (INSTANCE INTERNAL_SITE SITE IS2 (TRANSFORM MX))
      (INSTANCE INTERNAL_SITE SITE IS3 (TRANSFORM R180))
      (INSTANCE INTERNAL_SITE SITE IS4 (TRANSFORM MY))
      (COMMENT “SINCE THE ORIGIN (POINT 0 0) OF THE SITES”
       “AND THE MACROS IS IN THE UPPER RIGHT CORNER, IS1 -”
       “NORMAL ORIENTATION - IS THE LOWER LEFT SITE”))))

(CELL OUTPUT_DRIVER_QUAD_SITE
  (VIEW SYMBOLIC SITE
    (INTERFACE (BODY
          .
          .
          .
      (INSTANCE OUTPUT_DRIVER_SITE SITE ODR4 (TRANSFORM MY)))))
(CELL INTERNAL_SITE (COMMENT “INTERNAL ARRAY SITE”)
  (VIEW SYMBOLIC SITE
    (INTERFACE (ARRAYRELATEDINFO ARRAYSITE (SOCKET)))))
(CELL OUTPUT_DRIVER_SITE
  (VIEW SYMBOLIC SITE
    (INTERFACE (ARRAYRELATEDINFO ARRAYSITE (SOCKET)))))
```

LISTING 4—PHYSICAL VIEW OF THE M212 MACROCELL

```
(CELL M212
  (VIEW SYMBOLIC PHYSICAL
    (STATUS (EDIFVERSION 1 0 0)(EDIFLEVEL 0)
      (WRITTEN (TIMESTAMP 86 03 06 17 48 38)
        (ACCOUNTING AUTHOR “MOTOROLA INC. – ASIC PRODUCT DIV.”)
        (ACCOUNTING PROGRAM “GDSTOMER VERS M0558.00.002.028 **03/03/86**”)
        (ACCOUNTING DATAVERSION “REV0000000000000000”)))
    (INTERFACE
      (BODY
        (USERDATA BORDER BORDER
          (FIGUREGROUP BODY_EXTENT
            (RECTANGLE (POINT -320 -400)(POINT 320 0)))))
      (PORTIMPLEMENTATION YD
        (FIGUREGROUP ROUTING_LEVEL_2 (DOT (POINT 0 -50))))
      (PORTIMPLEMENTATION SYD
        (FIGUREGROUP ROUTING_LEVEL_2 (DOT (POINT -304 -50))))
      (PORTIMPLEMENTATION YA
        (FIGUREGROUP ROUTING_LEVEL_2 (DOT (POINT 304 -70))))
          .
          .
          .
      (JOINED YD SYD)(DEFINE INPUT PORT (MULTIPLE A F C G B E H D J))
      (DEFINE OUTPUT PORT (MULTIPLE YD SYD YA YC YB))
      (ARRAYRELATEDINFO ARRAYMACRO
        (PLUG
          (SOCKETSET (INSTANCE INT SITE IS1)
            (INSTANCE INT SITE IS2 (TRANSFORM MY))(TRANSFORM MY))
          (SOCKETSET (INSTANCE INT SITE IS3 (TRANSFORM R180))
            (INSTANCE INT SITE IS4 (TRANSFORM MX))(TRANSFORM MY)))))))
```

Listings continued on pg 184

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CIRCLE NO 75

LISTING 5—PIN-GRID-ARRAY ASSOCIATION FOR THE M212 MACROCELL

```
(CELL PIN_GRID_ARRAY
 (VIEW SYMBOLIC PHYSICAL
 (INTERFACE
  (DEFINE INOUT PORT
   (MULTIPLE PIN_E1 PIN_D1 PIN_C1 PIN_D2 PIN_C2 PIN_E3 PIN_D3 PIN_B1
            .
            .
            .
   PIN_A2 PIN_C4)))
 (CONTENTS (INSTANCE MOTOROLA_M2500ECL_BASE_ARRAY PHYSICAL BP)
  (JOINED (QUALIFY P001 BP)PIN_C3)(JOINED (QUALIFY P002 BP)PIN_B1)
            .
  (JOINED (QUALIFY P119 BP)PIN_A2)(JOINED (QUALIFY P120 BP)PIN_B2))))
```

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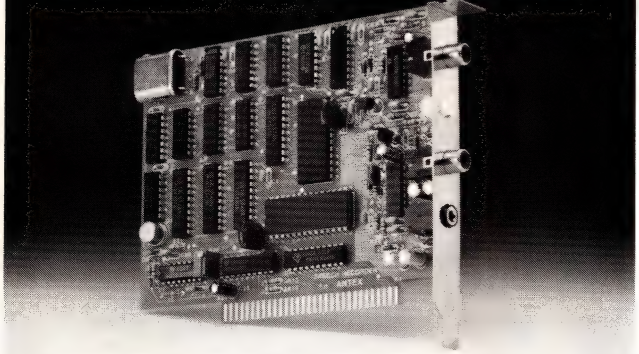

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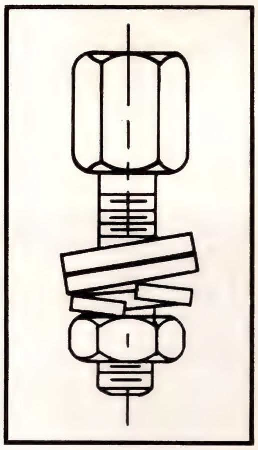

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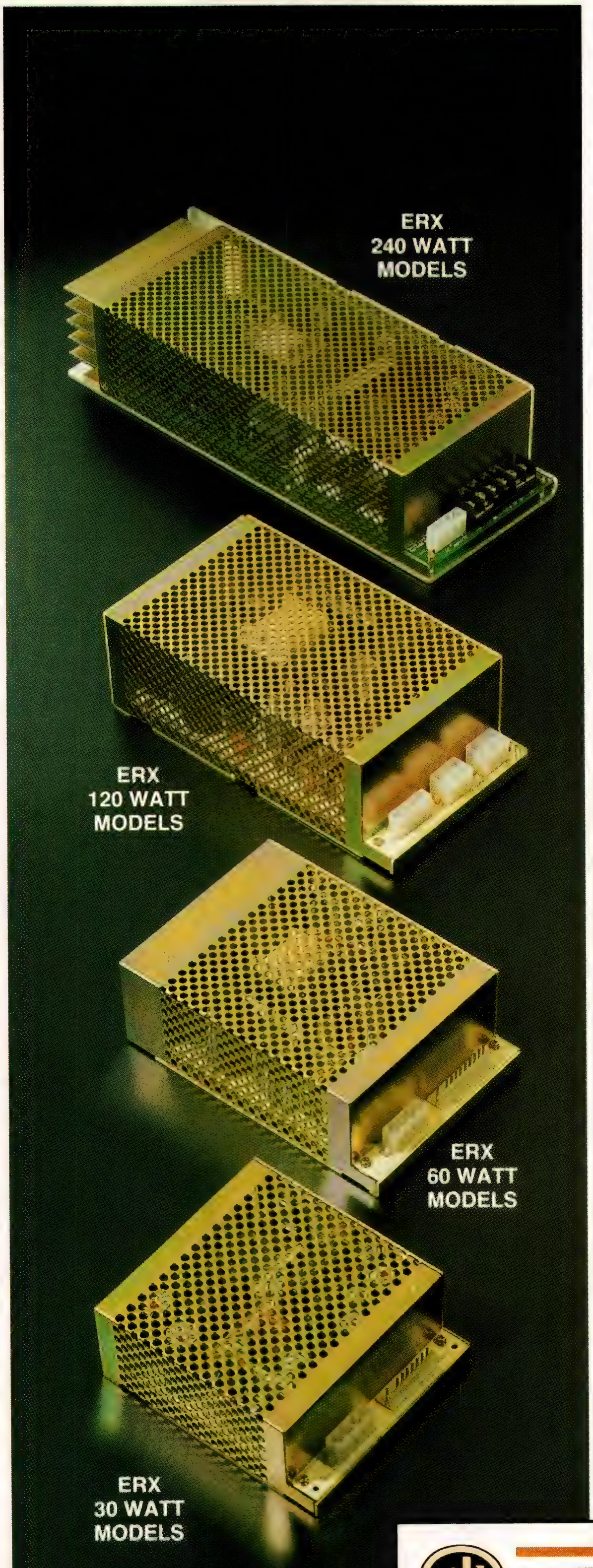

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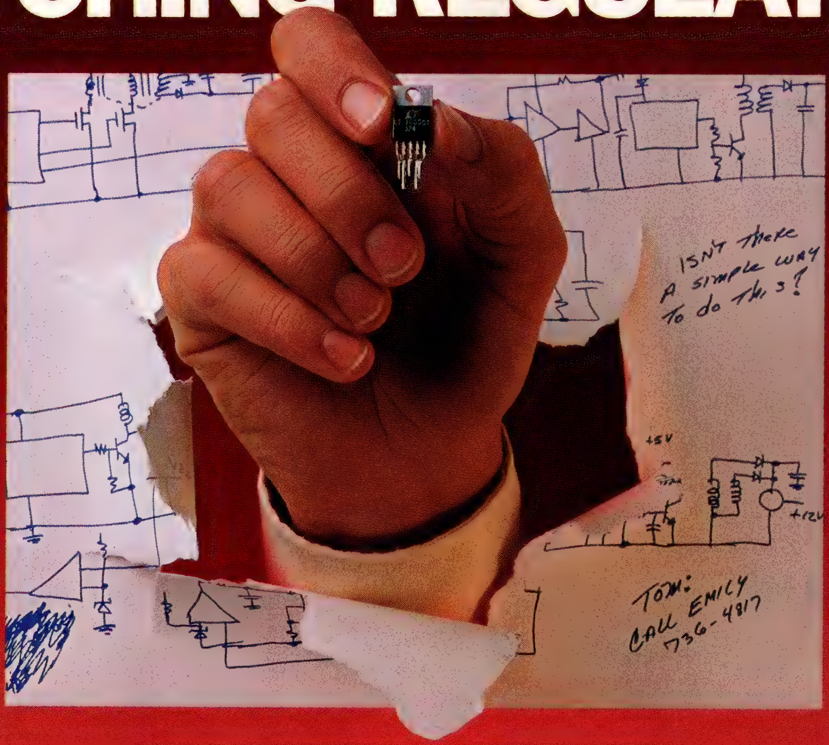

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The LT1070 family packs a real wallop by delivering load power up to 100 watts, with no external power devices, yet are extremely efficient even at low power levels. By utilizing current-mode switching techniques, these devices provide excellent AC and DC load and line regulation. They operate in nearly all switching topologies. And in the shutdown mode, the ICs draw only 50 μA supply current.

This highly versatile family operates over an extremely broad range of input voltages, load currents and switching configurations. Switching configurations include: buck, boost, flyback, forward, inverting, and "Cuk."

These regulators offer many unique features not found on vastly more difficult-to-use low-power control chips on the market. All devices use an adaptive, anti-saturation circuit for high switching efficiency and fast switching times. The LT1070 (and the LT1071/72 versions) are available in either standard 5-pin TO-3 or TO-220 power packages.

Take the sweat out of switching regulator design with the new LTC1070/71/72 family. Pricing for LT1070CT is $7.45 each in quantities of 100 (LT1071CT is $5.70 ea./100). The LT1072 will be available in the first quarter of 1987. For additional technical details, contact:
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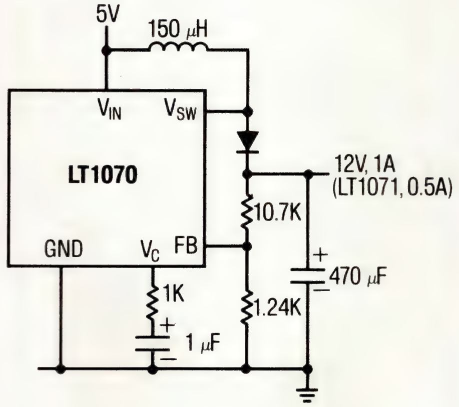

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CIRCLE NO 76

DESIGN IDEAS

EDITED BY TARLTON FLEMING

68008 µP uses 8259A for interrupts

David D Hyde
Goodyear Tire & Rubber Co, Akron, OH

For small systems, the 68000 or 68008 µP's autovector logic handles interrupts in a straightforward manner. You can implement a simple, level-triggered interrupt structure for these systems using a 74LS148 priority encoder and a few gates. This scheme doesn't readily allow expansion, though, nor does it allow the definition of dynamic vectors or the use of edge-triggered devices.

The 8259A interrupt controller can solve these problems, as users of 8086 peripherals can attest. Because the 68000 and the 8086 use externally generated, 1-byte interrupt vectors in the same manner, the shift register and gates **(Fig 1)** can transform the single 68008 interrupt-acknowledge bus cycle into two 8259A-compatible strobes. The penalty for this arrangement is a few CPU wait states.

The 68008's decoded interrupt-acknowledge signal ($\overline{\text{INTA68K}}$) must inhibit the data-transfer acknowledge signal ($\overline{\text{DTACK}}$) until the Q_6 output of shift register IC_4 goes high. At that time the $\overline{\text{INTA59A}}$ signal strobes IC_3, sending a valid interrupt vector to the µP on D_0-D_7. With software, you configure the 8259A as if it were operating in an 8086 system. If the application requires, you can cascade 8259As and support autovector operations as well. **EDN**

To Vote For This Design, Circle No 749

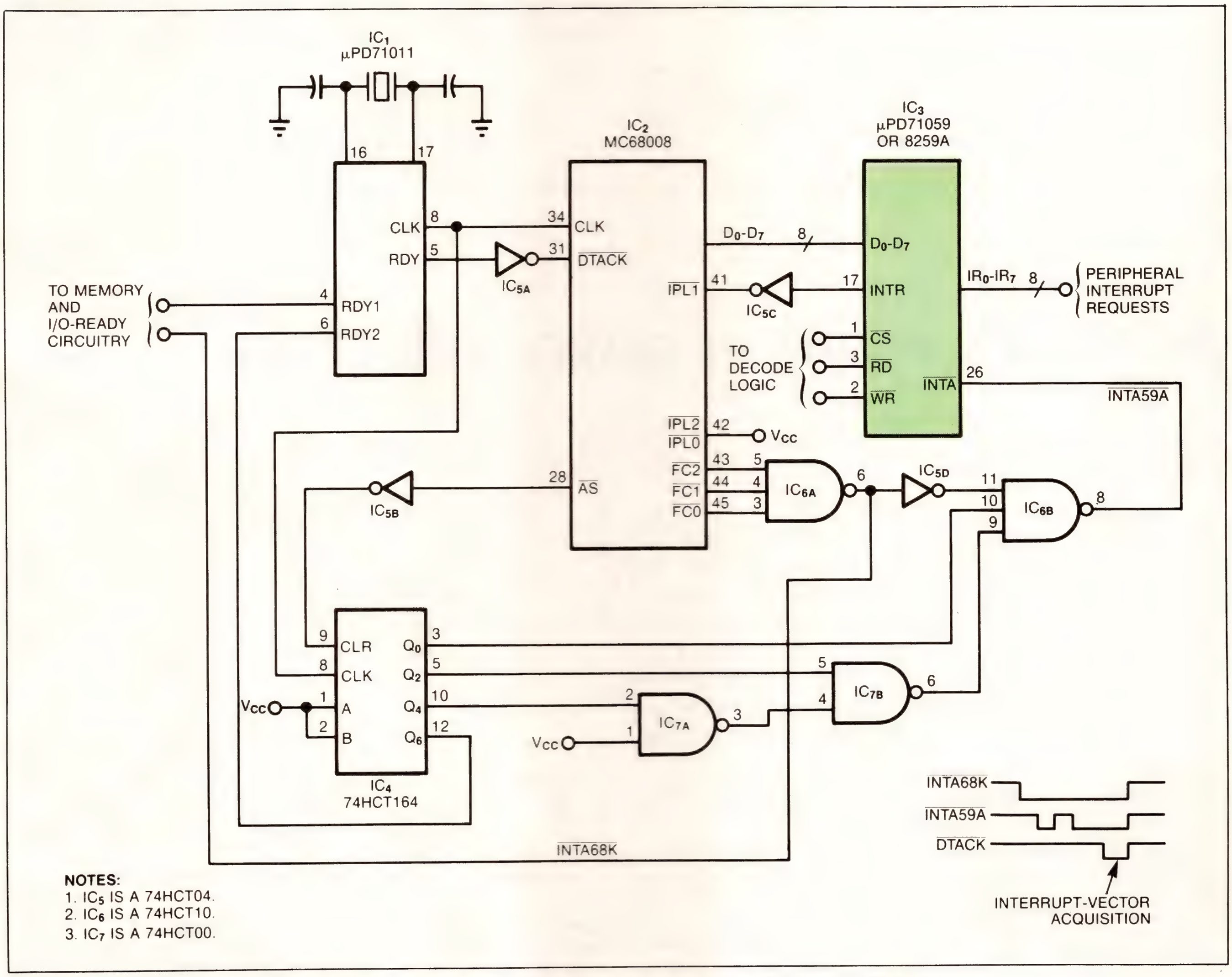


Fig 1—Using an 8086 peripheral (IC_3) in a 68000 system offers advantages over the µP's autovector logic.

MOSFET provides glitchless power backup

Tosh Mizuno
Dalmo Victor Co, Belmont, CA

The power-backup circuit of **Fig 1** switches from V_{CC} to the battery voltage without a glitch when V_{CC} power is lost. Q_1 acts as a current source during normal operation to provide the battery with a constant charge current. The loss of V_{CC} drops Q_1's gate voltage to 0V, which allows battery current to flow through the MOSFET's channel and integral body diode to the load.

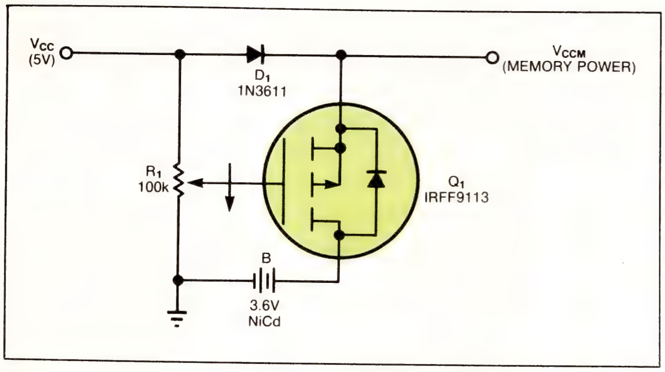


Fig 1—MOSFET Q_1 provides a constant charging current *to a battery during normal operation; the loss of V_{CC} turns Q_1 more fully on, delivering battery current to the load.*

For most p-channel MOSFETs, the gate-threshold voltage ranges from −2 to −4V, and thus Q_1 may not turn on fully for the 5V backup shown. As a result, V_{CCM} is nearly a diode drop less than the battery voltage. To back up higher values of V_{CC} (6 to 12V), use a higher battery voltage, so that Q_1 is fully on when its gate voltage drops to 0V. (V_{CCM} equals the battery voltage minus the product of channel resistance and load current.)

To calibrate this circuit, connect an ammeter in series with the battery. Then, with V_{CC} and the output load present, adjust R_1 for a battery-charging current slightly higher than that recommended by the manufacturer. **EDN**

To Vote For This Design, Circle No 747

Adjustable regulator covers wide range

Giovanni Stocchino and Angelo Tognoni
FATME, Rome, Italy

An adjustable regulator that offers precise control of current and voltage plus automatic crossover from one mode to the other is shown in the simplified diagram of **Fig 1.** Potentiometer R_V sets the regulated voltage; R_I sets the regulated current. This design avoids a compromise often required in voltage/current-stabilizer circuits, whereby a precise regulation of either current or voltage prevents a comparable regulation of the other quantity.

The precision op amp, IC_3, serves as a voltage follower and as a current sensor with near zero dropout voltage. By removing the load-current sensing operation from the voltage-regulation loop, the op amp allows the circuit to accomplish accurate regulation of both current and voltage; that is, IC_3 allows only the load current I_S to flow in its feedback resistor R_S while forcing V_{OUT} equal to the voltage to be regulated (V_{AB}).

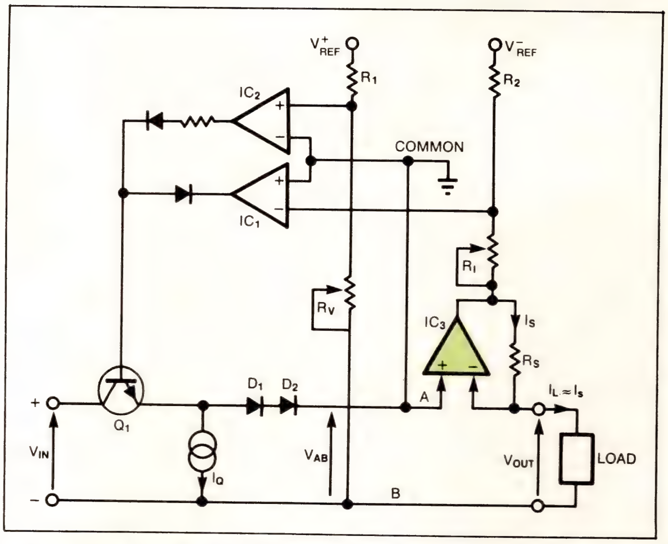
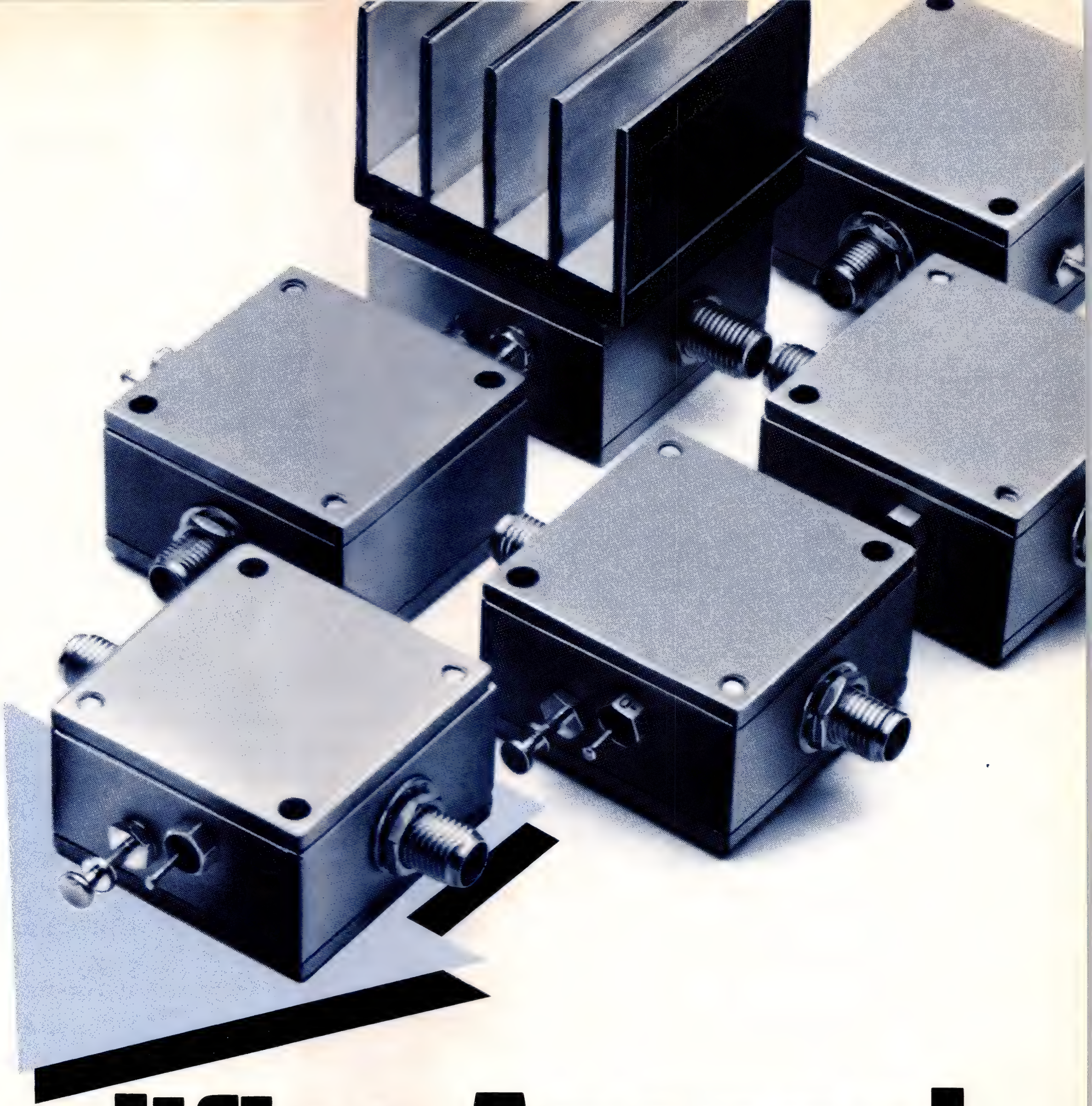


Fig 1—This adjustable regulator *uses separate control loops to stabilize voltage and current, and it provides an automatic crossover between those modes of operation. Potentiometers R_V and R_I let you adjust the regulated value of voltage (V_{OUT}) and current (I_S).*



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Gain (dB), Min.	20	17	20	28
Gain Flatness (dB) Max.	±1.0	±1.5	±1.5	±1.0
Max. Power (dBm) (1dB compression)	+10	+3	+17*	+20
NF (dB) typ.	5.3	12.0	7.0	5.0
3rd order Intercept pt (dBm)	+18	+13	+25	+33
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C101 REV. B

Therefore the following relationship holds true in the voltage-control mode:

$$V_{OUT}=V_{AB}+\epsilon_V=V_{REF}R_V/R_1+\epsilon_V,$$

where ϵ is the error voltage added to V_{AB}:

$$\epsilon_V=\pm V_{OS}-I_LR_S/A_0.$$

V_{OS} and A_0 are IC_3's input offset voltage and open-loop gain, respectively. Combining the guaranteed specs of an OP-07, for example, with the maximum value for I_SR_S (0.6V) yields, as an absolute value, $\epsilon_V \leq 27\ \mu V$ for any output voltage.

In the current-control mode,

$$I_L=I_S+\epsilon_I\approx V_{REF}R_I/(R_2R_S)+\epsilon_I,$$

and

$$\epsilon_I=\pm(I_{OS}+I_B/2),$$

where ϵ is the error contribution from IC_3, and I_B and I_{OS} are the respective input bias and offset currents of IC_3. Again, guaranteed OP-07 specs yield, as an absolute value, $\epsilon_I \leq 4$ nA, for any load current.

The current sink $I_Q > I_{CO}$ extends the lower limit of the output-current range to nearly zero by compensating for Q_1's cutoff current I_{CO}. Diodes D_1 and D_2 preserve the effect of this compensation for outputs near 0V.

Fig 2 shows a practical version of the circuit, which provides regulated outputs in the range of 0 to 300V and 10 nA to 20 mA. Accuracy and drift are virtually the same as that of the REF-05 regulator (IC_5). The additional components (compared to **Fig 1**) enhance resolution and reliability.

For example, D_8-D_{13} protect the op-amp inputs from overload. The frequency-compensation components are C_1, R_6, C_2, and R_7 in the voltage loop and C_3 and R_{10} in the current loop. Q_4 boosts the output-current capability of IC_4. Q_3, D_1, D_2, and R_2 make up the current sink (shown as I_Q in **Fig 1**). To offset any loss of reliability caused by slow response in the main current-control loop, Q_2 and R_1 form a fast control path for output current that also limits Q_1's emitter current to about 30 mA. The switch-selectable ranges provide fine adjustment for output current (S_1) and voltage (S_2). **EDN**

To Vote For This Design, Circle No 748

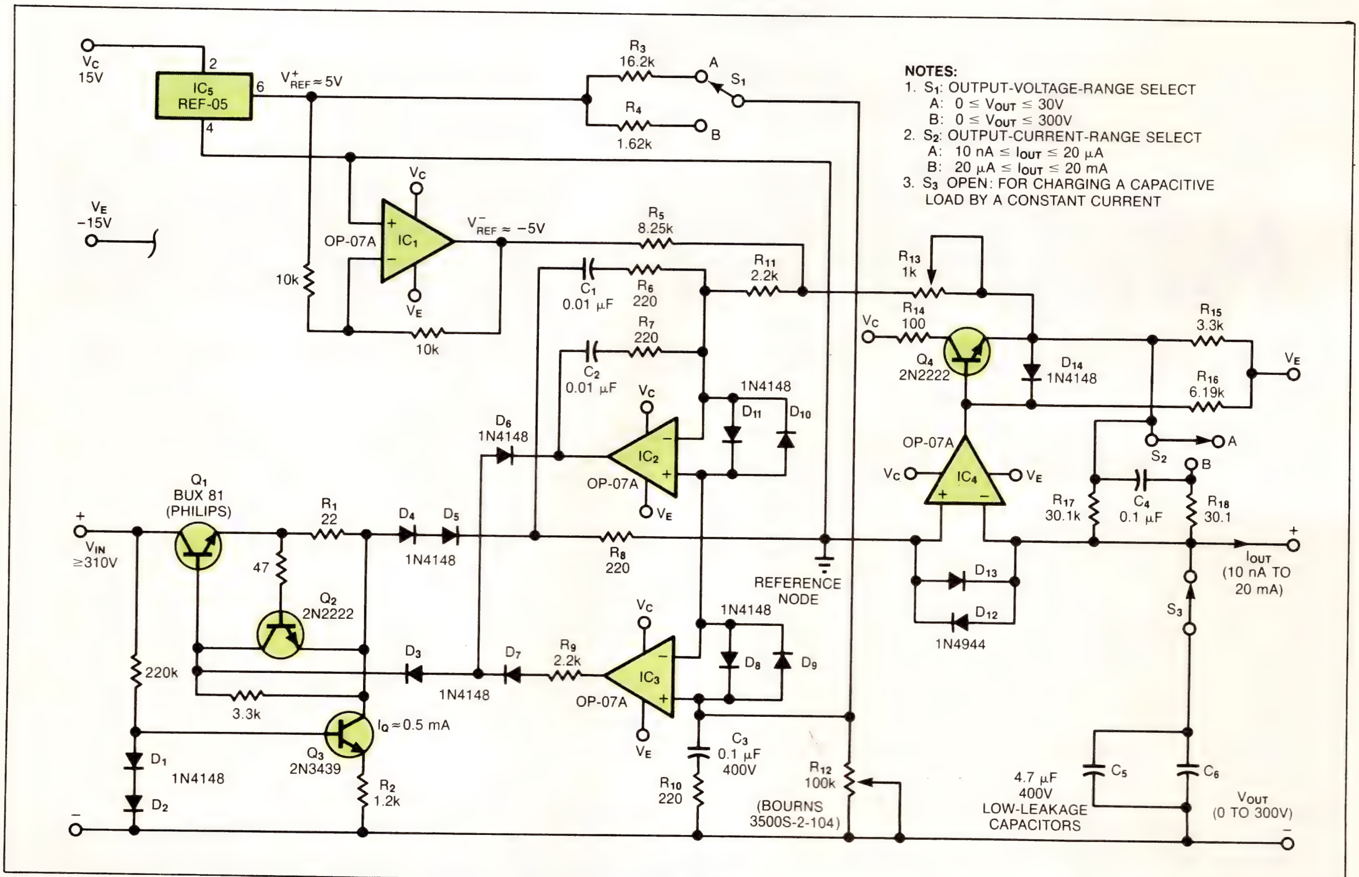

***Fig 2—Additional components give this regulator circuit** more resolution and reliablility than the one in **Fig 1**. Potentiometers R_{12} and R_{13} let you set regulated voltage and current levels in the ranges of 0 to 300V and 10 nA to 20 mA.*

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CIRCLE NO 79

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µP controls serial D/A converter

Daniel A Heuer
Magnavox, Fort Wayne, IN

A microprocessor can generate analog voltages via an I/O port using the minimum-hardware approach of **Fig 1.** The µP simply sets the data line high; activates the inverter's output by asserting a high logic level on the 3-state control line; writes one controlled-duration data pulse; and returns the inverter output to its high-impedance state.

The µP can then continue with other processing, repeating this refresh operation only at irregular intervals. Each refresh drives V_{OUT} closer to the desired value. The output settling time depends on the conditions of your application: frequency of refresh, values of R and C, and load resistance. (Low-resistance loads require more frequent refresh operations to maintain the output level.) This conversion technique eliminates the need for precise timing except for the generation of one pulse width within a short subroutine—a task the µP can easily handle. **EDN**

To Vote For This Design, Circle No 746

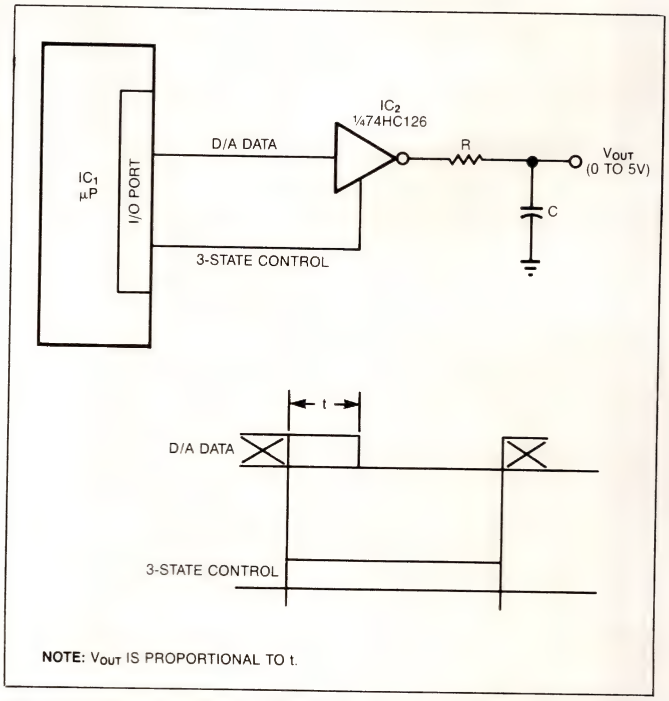

***Fig 1—In this minimum-hardware D/A converter,** the capacitor charges to the desired output voltage by integrating a series of controlled-duration pulses.*

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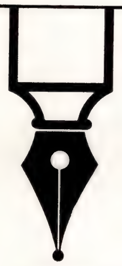

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DESIGN IDEAS

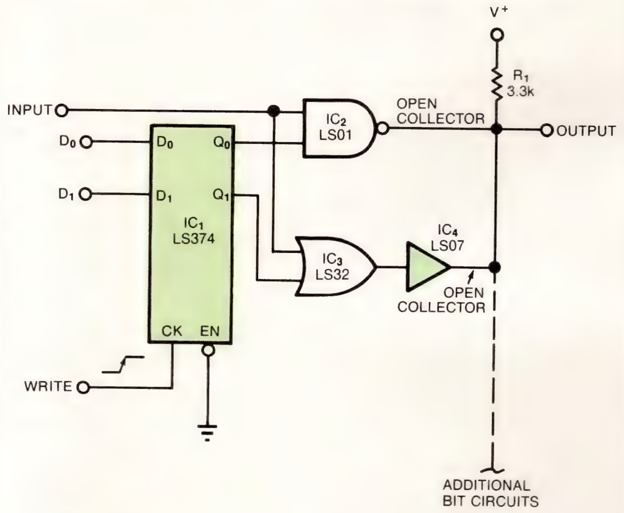
Circuit recognizes real-time data

Ted Sabat
Allen Bradley, Highland Heights, OH

You can program the 1-bit circuit in **Fig 1** to qualify a clock signal in a μP-based system. Alternatively, you can perform high-speed data recognition on n-bit parallel words using n of these circuits with the outputs tied in parallel to the common pullup resistor (R_1). Software can direct a μP to do these tasks, of course, but the hardware approach is much faster.

First, the μP system sets the desired qualifying condition (high, low, don't care, or never) by writing bits D_0 and D_1 to the latch, IC_1. Then, the input signal and the latch outputs (Q_0 and Q_1) control the output as shown in the truth table. (The output goes high when the circuit recognizes an input state but remains low otherwise.) All gates tied to the pullup resistor must have open-collector outputs; thus, the circuit includes IC_4 to provide an open-collector or gate, a function not readily available. **EDN**

To Vote For This Design, Circle No 750



Q_1	Q_0	FOR OUTPUT HIGH, THE INPUT MUST BE:
0	0	1
0	1	NEVER (OUTPUT IS ALWAYS LOW)
1	0	DON'T CARE (OUTPUT IS ALWAYS HIGH)
1	1	0

***Fig 1—This circuit performs real-time recognition** of one or more bits according to one of four qualifying conditions.*

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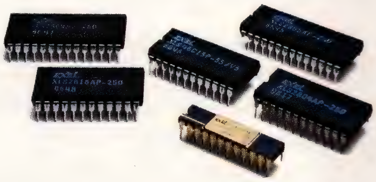

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Datacopy Corp, 1215 Terra Bella Ave, Mountain View, CA 94043. Phone (415) 965-7900.

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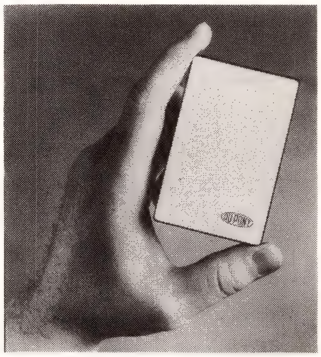
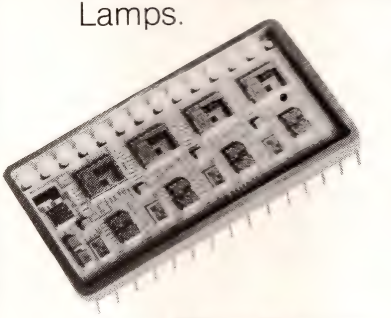
MEMORY CASSETTES

- *Removable RAM cassettes*
- *Power source included in the cassette*

You can obtain memory cassettes with capacities as high as 1M bit of static RAM in compact styles designated as CC (credit card), M (miniature), and S (standard). Each device consists of a 2-part system: a cassette that resides in the host equipment and has an integral connector and mating header. A pin-and-socket connector, which withstands 10,000 mating cycles, connects the host to the cassette. The connector is packaged on 0.05-in. centers to accommodate high-density, high-performance printed-circuit technologies. The 1M-bit CMOS static RAM memory consists of sixteen 64k-bit chips mounted on a chip-on-board array within a 0.12-in.-thick plastic case. The 38 contacts are mechanically shielded. Header pins for the interface are designed for through-hole mounting to pc boards. The cassette includes a replaceable 3V battery that operates for 2.5 years min. The 1M-bit cas-





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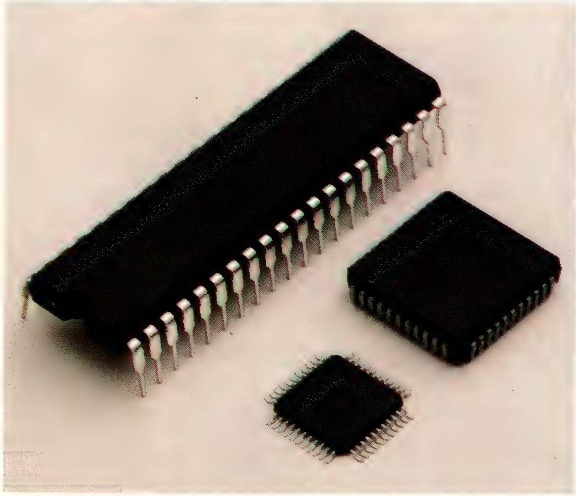

The V20/V30 are powerful CMOS microprocessors providing high-speed performance at vastly reduced power consumption. Internally 16-bit, the V20 has an 8-bit external bus, and the V30 is a full 16-bit machine. Both feature NEC's unique dual bus architecture, two program counters, and a super-efficient address generation logic, making them up to 50% faster. Low heat dissipation allows flexible plastic or ceramic-based packaging in three different configurations.

Pin compatible with µPD8086/88 devices, the V20/V30 incorporate an enhanced instruction set giving that extra performance edge required by time-critical applications. A complete range of compatible CMOS peripherals keeps engineering effort to a minimum. Heavy computational loads will be catered for by a CMOS floating point processor. There is a choice of 5,8 and 10 MHz clock rates for different operating environments.

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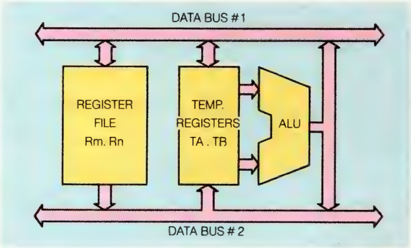
µPD71055	Parallel interface unit
µPD71059	Interrupt control unit
µPD71071	DMA controller
µPD71011	Clock pulse generator/driver
µPD71082/83	8-bit latch
µPD71086/87	Bus driver/receiver
µPD71088	System bus controller

Compatibility of development tools safeguards investments and provides familiar and time-proven methods of reaching powerful new solutions. NEC support software includes an in-circuit emulator package, relocatable assembler plus a C-Compiler µPD8086/88 code written for both the Small and Large model can be run without modification on the V20/V30. The migration path to the V40/V50 microprocessors underlines NEC's overall V-Series software compatibility strategy. In addition, the V20/V30 are supported by development systems from Hewlett-Packard and Tektronix. NEC's V-Series devices are secondsourced by Zilog and Sony.



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sette, $200.

Du Pont Connector Systems, 515 Fishing Creek Rd, New Cumberland, PA 17070. Phone (717) 938-7589.

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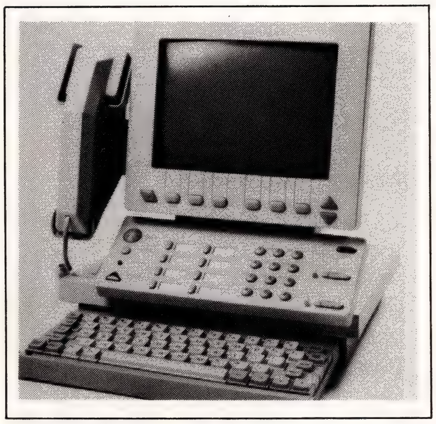

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Cermetek Microelectronics Inc, 1308 Borregas Ave, Sunnyvale, CA 94088. Phone (408) 752-5000. TWX 910-379-6931.

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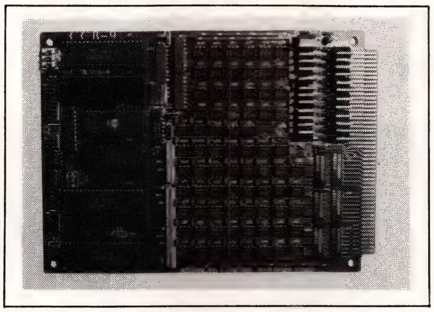

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Advanced Control Systems Corp, 205 Oak St, Pembroke, MA 02359. Phone (617) 826-4477.

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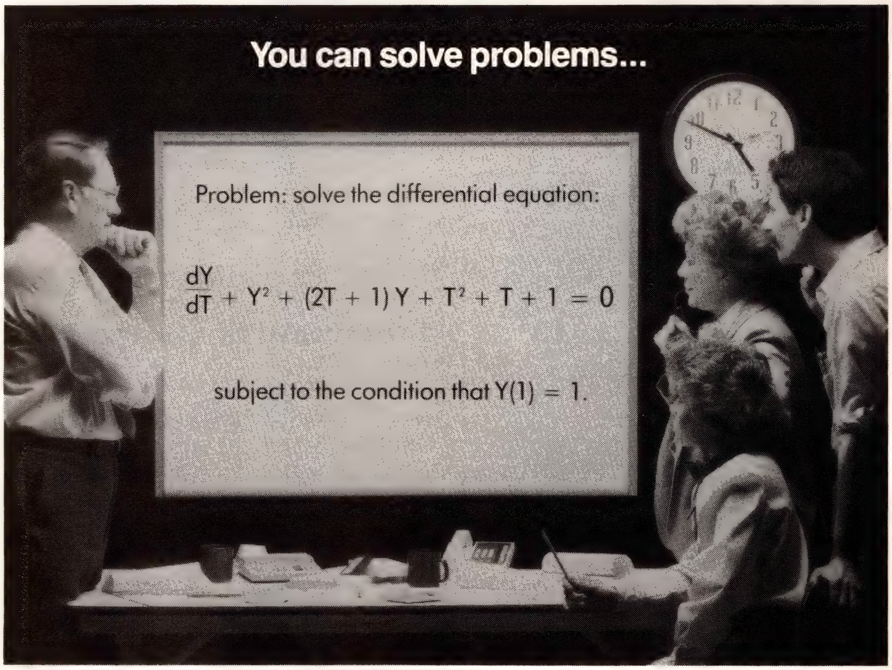

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subject to the condition that Y(1) = 1.

Symbolically...

```
(C1) DEPENDS(Y,T)$
(C2) DIFF (Y,T) + Y ^2 + (2*T + 1)*Y + T ^2 + T + 1;
         dY     2                  2
(D2)     --  + Y  + (2 T + 1) Y + T  + T + 1
         dT
(C3) SOLN:ODE(D2,Y,T);
                        T
                 %C T %E  - T - 1
(D3)     Y = -  ------------------
                          T
                    %C %E  - 1
(C4) SOLVE(SUBST([Y = 1, T = 1],D3),%C),NUMER;
(D4)     [%C = 0.5518192]
(C5) SPECIFIC_SOLN:SUBST(D4,SOLN);
                             T
             0.5518192 T %E  - T - 1
(D5) Y = -  ------------------------
                              T
                 0.5518192 %E  - 1
```

and Numerically.

```
(C6) FORTRAN(D5)$
        Y = -(0.5518192*T*EXP(T) - T - 1)
   1          /(0.5518192*EXP(T) - 1)
```

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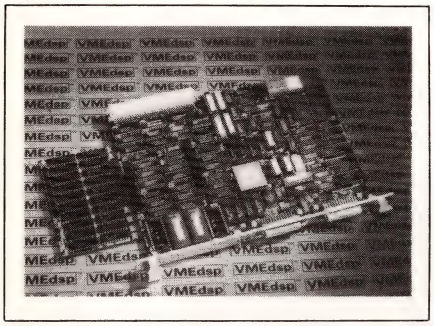
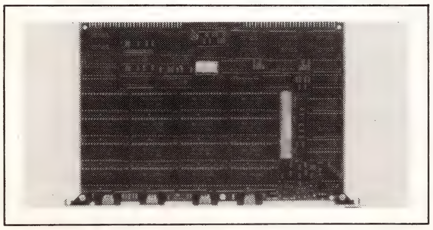


standard, including revision C.1. It features A24, D16, and slave configurations and seven vectored-interrupt levels. You can select data in blocks of 16M bytes via addresses, and you can expand program memory from 16k bytes of zero-wait-state PROM to 128k bytes. Both the global-data memory and local-data memory can expand from 32k to 64k bytes of RAM. The ACX120 plug-in memory expansion module adds 96k bytes of program RAM, 32k bytes of global-data RAM, and 32k bytes of local-data RAM. SPV120, $2495; ACX120A with 32k bytes of program RAM, $395; ACX120B with 160k bytes of RAM, $1495.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

Circle No 355



MEMORY BOARD

- *Board offers 512k bytes or 1M byte of dual-port static RAM*
- *Lithium batteries provide backup*

The SRAM-3 memory board is a VME Bus/VMX Bus board that provides nonvolatile storage of 512k bytes or 1M byte in dual-port static RAMs. The company guarantees that the backup lithium cells will retain data for as much as 6000 hours for the 1M-byte version or 10,000 hours for the 512k-byte version. Sensory circuitry is set to detect a voltage level of 4.65V or less on V_{CC}; at this point the chip-enable and -select signals to the RAMs are driven in an inactive mode, and the power-down mode of the static RAMs is activated in order to prevent data corruption. The dual-port memory and onboard arbitration logic lets you establish two memory areas, to be selected for VME Bus access only, for VMX Bus access only, or for both. You set jumpers to determine access-base addresses and address-modifier codes. Arbitration logic (35-nsec overhead) and latched address and data buses enable the interleaving of write operations, ensuring a sustained data throughput of 16M-bytes/sec. SRAM-3A, $2650; SRAM-3B, $4150.

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410.

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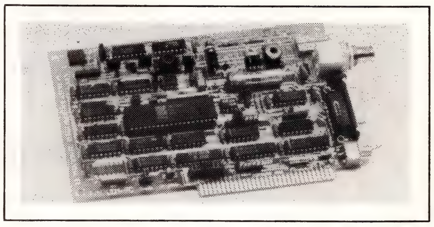

MEASURING SYSTEM

- *Distance-measurement board for IBM PC*
- *Uses ultrasonic transducer for noncontact measurement*

The UDM-PC ultrasonic distance-measurement board requires one expansion slot in an IBM PC; it uses a remote transducer to measure the distance to target objects. You can expand your system to 14 distance-measurement channels by using external multiplexing. The board and the off-board transducer measure distances between 5 in. and 35 ft and are suitable for use in noncontact measurement applications, such as materials dimensioning, solid or

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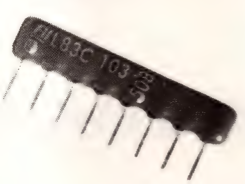

For applications assistance or the **BI** Resistive Products Short Form Catalog, call **(714) 447-2700.**

POTS/DIALS

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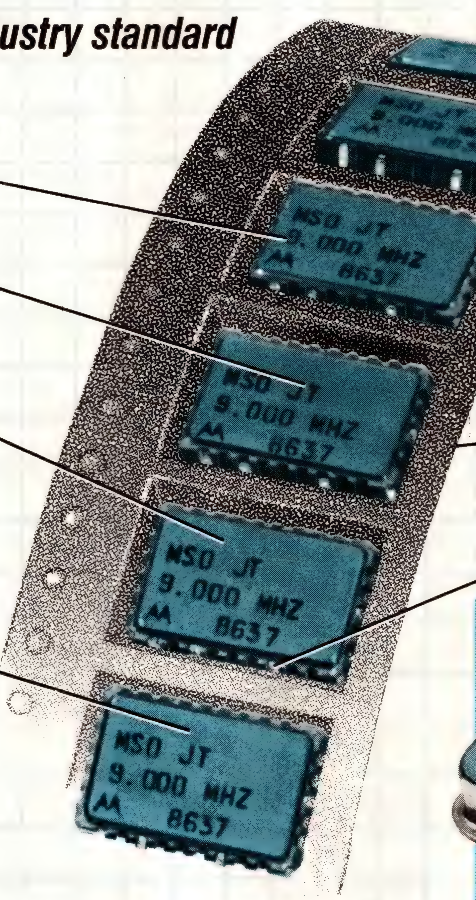
CIRCLE NO 34

Surface Mount Oscillators from Motorola

. . . the new industry standard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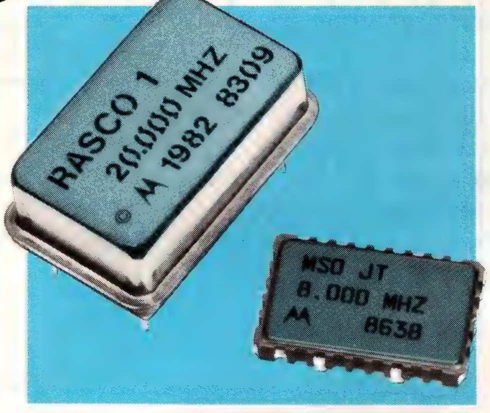
ANTI-STATIC TUBE PACKAGING OR 24 mm TAPE & REEL
1.5 TO 35 MHz FREQUENCY RANGE
CMOS OR TTL COMPATIBLE
VAPOR PHASE/WAVE SOLDER PROCESS
CUSTOM IC CHIP, FEWER COMPONENTS, FEWER INTERCONNECTS
7" REEL (300 PCS) OR 13" REEL (1200 PCS)
OPTIONAL ENABLE/DISABLE WITH CMOS OR TTL
"C" LEADS STANDARD 0.125" (3,18 mm) SEATED HEIGHT
"J" LEADS OPTIONAL 0.160" (4,06 mm) SEATED HEIGHT
PROPRIETARY AT STRIP CRYSTAL WITH EXCELLENT SHOCK PERFORMANCE
45/55% SYMMETRY OPTIONAL
MSO JT
9.000 MHZ
AA 8637



Motorola's RASCO oscillator and the New Surface Mountable MSO

Ideal for Automatic Placement — Motorola's MSO Series oscillators are designed for placement with state-of-the-art pick-and-place automated assembly equipment and are available with either tape & reel or anti-static tube packaging. The MSO oscillator is vapor phase/wave solder reflowable.

Product Features — Available over a frequency range of 1.5 MHz to 35 MHz, with stability of ±0.01% over the temperature range of 0°C to +70°C. Symmetry is 40/60% standard, with 45/55% optional. Compatible with either CMOS or TTL logic.

5,000g Shock Rating — Uses AT strip crystals with mechanical shock performance greatly superior to that of conventional crystals — made by a proprietary process that avoids the edge faults, fractures, and weaknesses inherent to conventional processes.

A New Quality Standard — Even when compared to the industry standard RASCO clock oscillators, MSO Series oscillators have 59% fewer processing operations, are assembled in a class 100 clean room with completely automatic processing, have 37% fewer components and 58% fewer interconnects.

For additional information or for samples, contact Motorola Inc., Components Division, Data Clock Sales, 2553 N. Edgington St., Franklin Park, IL 60131, or call (312) 451-1000, Ext. 4835, FAX: (312) 451-7585 TWX: (910) 255-4619 TELEX: 499-0104.

MOTOROLA

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Motorola Components Division is a broad-based supplier of quality components for the electronics OEM. For more information about specific product lines, contact:
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NiCd Batteries / Ft. Lauderdale, FL (305) 475-5000 • **Printed Circuit Boards** / Schaumburg, IL (312) 576-8468

CIRCLE NO 62

liquid level measurement, recognition and positioning of objects, proximity sensing, and security. The absolute accuracy of the device is ±0.015 in. and the resolution between targets is ±0.27 in. within 5 ft. You can program distance parameters so that the system will discriminate among targets. In local mode, the board checks its own ranging facilities. $695.

ICS Computer Products Inc, 5466 Complex St, Suite 208, San Diego, CA 92123. Phone (619) 279-0084.

Circle No 357

PRINTER UPGRADE

- *Upgrade kit for HP printer line provides 2M bytes of RAM*
- *Enables printer to print full-page, 300-dpi graphics*

The 2M-byte upgrade kit for the Laserjet, Laserjet Plus, and Laserjet 500 Plus printers replaces the printers' main interface boards and provides 2M bytes of RAM. The RAM expansion allows the printers to print full-page, 300-dpi graphics; you can also download more fonts for desktop-publishing applications. The upgrade board incorporates the company's PCL (Printer Control Language), so software that's currently available for the printer family is compatible with the board. $2495.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 358

LAN ACCESSORY

- *Provides connection to a number of LANs*
- *Directed at IBM networks*

Using the company's NonStop systems and its Multilan products, you can connect to any validated IBM PC-based LAN that supports the IBM Network Basic Input/Output System (NETBIOS) protocols. Multilan is a means to integrate IBM PCs through a variety of LANs. Multilan products provide connections to IBM token-ring, IBM PC network, Ungermann-Bass Net/One, and Systek System 6000; all these LANs, as well as others, have adopted the NETBIOS programmatic interface, which provides an interface between programs executing in a workstation and an attached LAN. Multilan controller, $4000; Multilan attachment device, $4000; Multilan access method and file server, $6400.

Tandem Computers Inc, 19333 Vallco Parkway, Cupertino, CA 95014. Phone (408) 725-6000.

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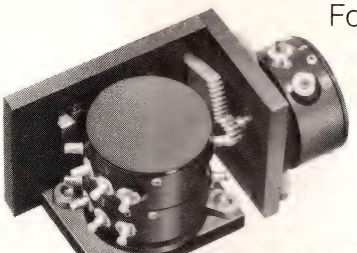

Beckman Industrial™

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CIRCLE NO 35

NETWORKS

EDN REPRINTS

A Designer's Guide to:

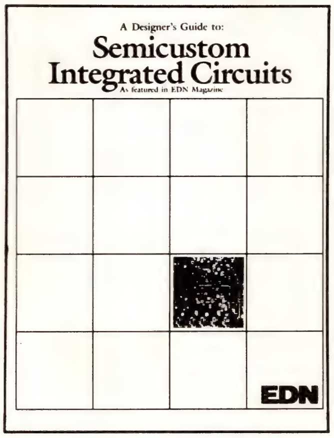
CMOS ICs

As featured in EDN Magazine

EDN

A Designer's Guide to CMOS ICs

CMOS is fast becoming the chosen technology for developing integrated circuits. That's because CMOS ICs are able to implement ultra-complex system-level functions on a chip! Now you can meet the special challenges posed by this new breed of ICs with *A Designer's Guide to CMOS ICs.* You'll learn the advanced design and fabrication techniques required. Plus the latest linear and digital CMOS ICs available.


A Designer's Guide to:

Semicustom Integrated Circuits

As featured in EDN Magazine

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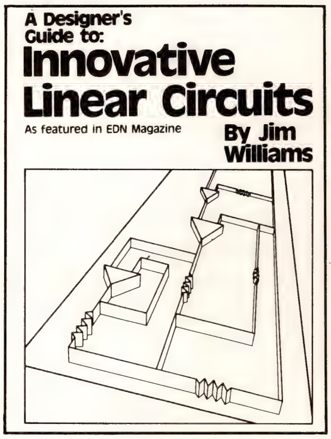
A Designer's Guide to Semicustom Integrated Circuits

Learn how to design a semicustom IC with *A Designer's Guide to Semicustom Integrated Circuits.* Based on EDN's own design experience, this nine-chapter booklet outlines the complete procedure used to design, fabricate, and test EDN 1, a chip with a 1200 equivalent-gate complexity. You'll not only learn the steps to take when creating ICs, but also the design/cost analyses and vendor-interface methods that lead to successful semicustom chips.


A Designer's Guide to:

Innovative Linear Circuits

As featured in EDN Magazine

By Jim Williams

A Designer's Guide to Innovative Linear Circuits

As exciting as digital technology is, you still need analog circuitry to operate on signals from real-world sources. Now, EDN is offering a wealth of analog design information in *A Designer's Guide to Innovative Linear Circuits.* This 186-page collection of articles was developed by Jim Williams, one of America's foremost linear-circuit designers. It includes practical and efficient ways to use op amps, comparators, data converters, and other analog ICs, and discusses the theories behind all the design techniques presented.

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EDN 2587

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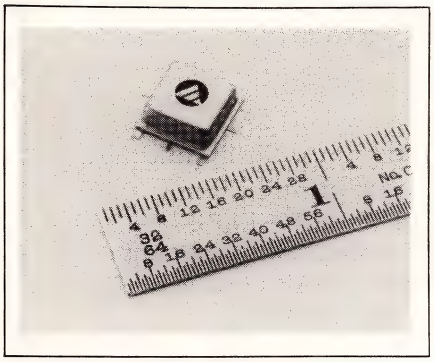
COMPONENTS & POWER SUPPLIES



AMPLIFIER

- *Minimum gain equals 10 dB*
- *Maximizes component density on microstrip pc boards*

The PPA-1043 PlanarPak surface-mount amplifier has a minimum gain of 10 dB (10.5 dB typ) over a 10- to 1000-MHz range. The amplifier's 0.375×0.375-in. package maximizes component density on microstrip pc boards, and it has a maximum noise figure of 4 dB (2.5 typ). The minimum 1-dB-compressed output power equals 6 dBm (8 dBm typ). The maximum input and output VSWR specs at 2:1 (1.7:1 typ). All specs are fully guaranteed over a 0 to 50°C operating range; slightly reduced specifications apply over the −55 to +85° military range. $175.

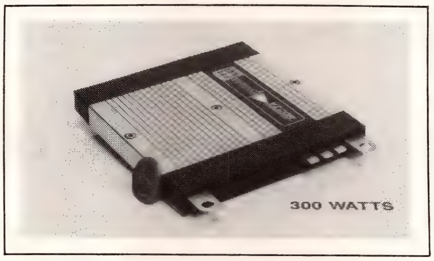
Avantek Inc, 3175 Bowers Ave, Santa Clara, CA 95054. Phone (408) 970-2583.

Circle No 360

DC/DC CONVERTERS

- *Feature 20W/in³ power density*
- *Meet UL, CSA, and VDE safety specifications*

Units in the MegaModule Series offer 5, 12, 15, 24, and 48V outputs at 300W. All outputs are adjustable from zero to 10%. The series offers four input ranges: 24V nominal (19 to 30), 48V nominal (40 to 60), 135V nominal (100 to 200), and 270V nominal (200 to 400). The converters meet UL, CSA, and VDE safety specifications. They use a proprietary phased-array architecture that drives two 150W power trains 180° out of phase. The effective operating frequency is 2 MHz. Efficiency specs at 80% for 5V models, 84% for 12 and 15V models, and 86% for 24 and 48V units. Other features include current limiting, thermal shutdown, overvoltage protection, remote sensing, and 3750V ac input-to-output isolation. The line regulation equals 0.1%, and the load regulation (from 10% to full load) is 0.2%. The operating range, with no derating, equals −20 to +85°C. $265 (OEM qty). Delivery, six to eight weeks ARO.



Vicor Corp, 23 Frontage Rd, Andover, MA 01810. Phone (617) 470-2900. TWX 910-380-5144.

Circle No 361

DC/DC CONVERTERS

- *Tested to MIL-STD-202*
- *Efficiencies as high as 70%*

This line of dc/dc converters includes single- and dual-output, nonisolation polarity-reversing and nonisolation voltage-boosting units; 48V dc telecomm multiple-output devices; and isolation-type models with outputs of 0.3 to 3W. All units are tested to meet MIL-STD-202 and offer efficiencies as high as 70%. The four 5V-input polarity-reversing units provide outputs of −5 or −12V dc. Nonisolation voltage-boosting converters offer outputs of 12, 15, or 24V dc from a 5V dc input. Isolation-type converters are

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CIRCLE NO 36

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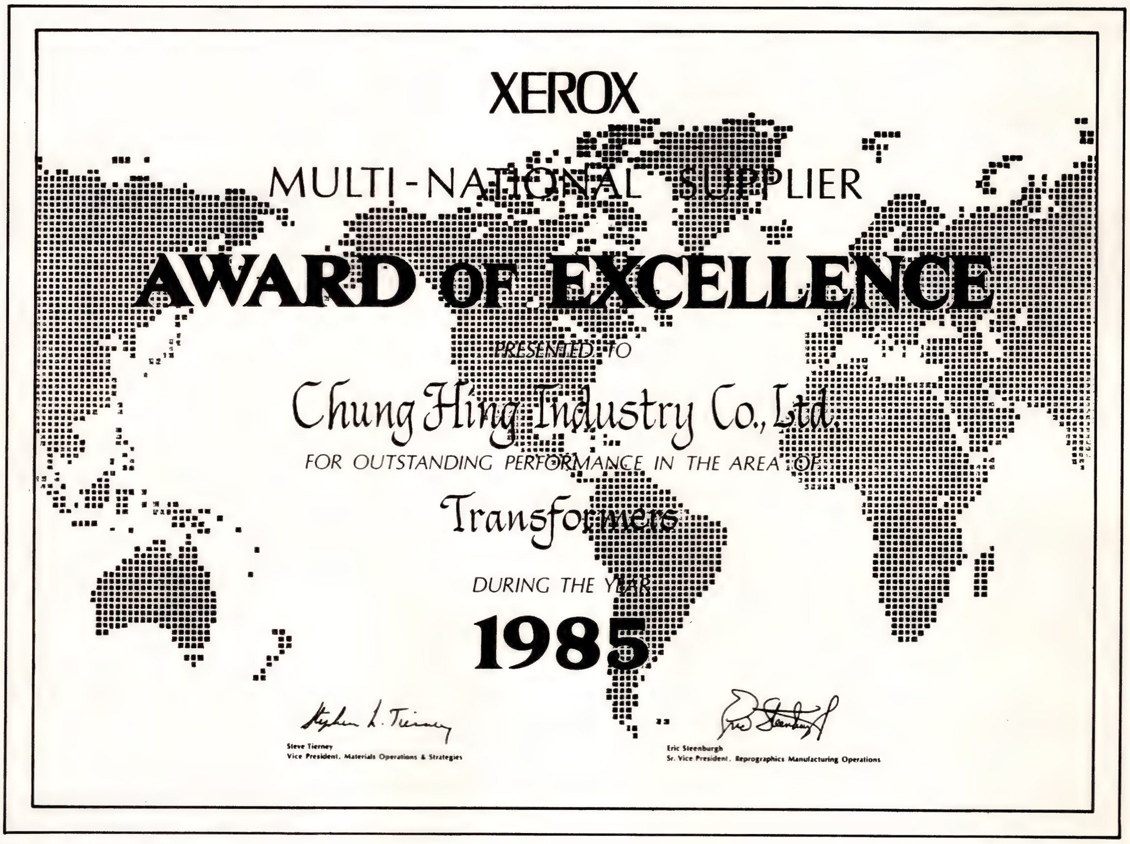
Thanks to Xerox Corporation again !!!!!

The Board of Directors
Chung Hing Industry Co., Ltd.
17 October, 1986



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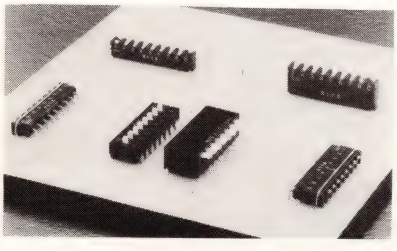
grouped in power ranges of 0.3, 0.5, 1, and 3W in single- and dual-output models. Telecomm converters provide ±5 and ±12V dc from a 48V dc input. $7 to $16.

Pan-Magnetics International Inc, 455-C Carson Plaza Dr, Carson, CA 90746. Phone (213) 532-1790.

Circle No 362



SWITCHES

- *Available in two heights*
- *Feature gas-tight contacts*

S Series SIP switches take up less than 50% of the board space required by conventional DIP switches. They are available in 0.295- and 0.177-in. heights; both configurations are also available in right-angle versions that stand just 0.16 in. off the board. All versions are available as 2-, 4-, 6-, 8-, or 10-position switches and use high-pressure gas-tight contacts that accommodate wave-solder operations and aqueous or solvent cleaning. Lifetime specs at 1000 cycles. An 8-position switch, $0.98 (10,000).

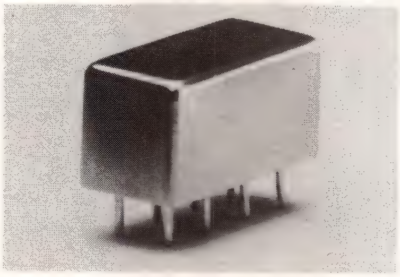
Alco Electronic Products Inc, 1551 Osgood St, North Andover, MA 01845. Phone (617) 685-4371. TWX 710-342-0552.

Circle No 363

PHASE DETECTOR

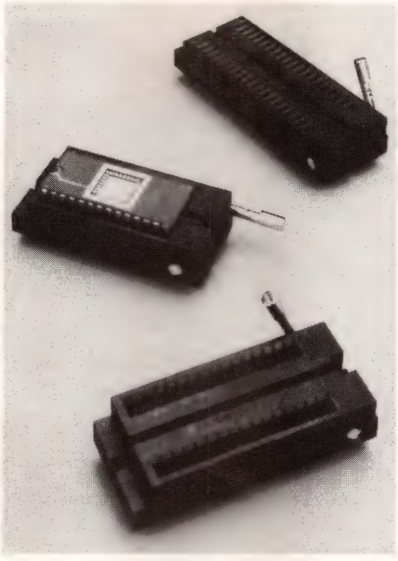
- *Delivers 1000-mV output*
- *Housed in hermetically sealed, EMI-shielded metal case*

The MPD-2 operates over a 10- to 2000-MHz range. With 7 dBm applied to the LO and RF ports, it delivers a 1000-mV output to provide a figure of merit of 143. Output and input impedances equal 50Ω. The detector comes in a hermetically sealed, EMI-shielded metal case measuring 0.2×0.5×0.25 in. Isolation specs at 40 dB min. The detector's output is negative, and the dc-offset voltage is 0.3 mV typ. $20.95 (5).



Mini-Circuits, Box 166, Brooklyn, NY 11235. Phone (718) 934-4500.

Circle No 364



DIP SOCKETS

- *Rated for use at 150°C*
- *Life specs at 100,000 cycles*

DIP III zero-insertion-force sockets are designed for test and burn-in service. They are rated for use at 150°C in burn-in applications. For programming applications with standard DIP devices, the sockets have a minimum life of 100,000 cycles. The sockets are available in 24-, 28-, 32-, and 40-lead versions.

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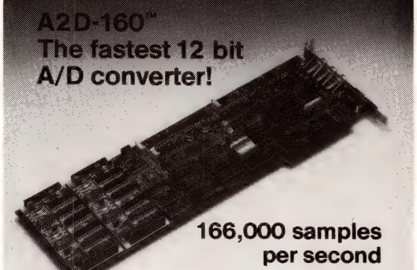
For the IBM PC, XT and compatibles



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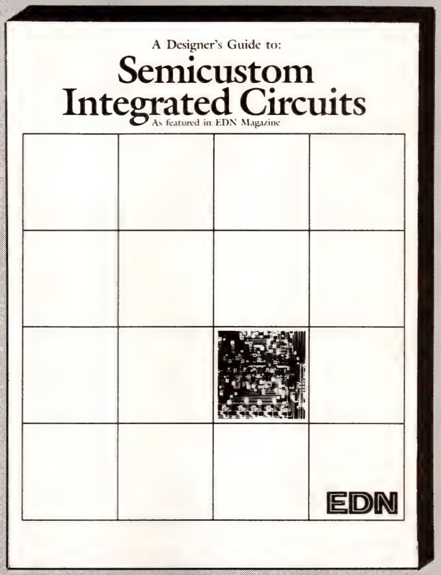
02364 USA
(617) 746-7341

CIRCLE NO 37

You are only nine chapters away from understanding Semicustom IC design



Learn how to design a semicustom IC with *A Designer's Guide to Semicustom Integrated Circuits.* Based on EDN's own design experience, this nine-chapter booklet outlines the complete procedure used to design, fabricate, and test EDN 1, a chip with a 1200 equivalent-gate complexity. You'll not only learn the steps to take when creating ICs, but also the design/cost analyses and vendor-interface methods that lead to successful semicustom chips.

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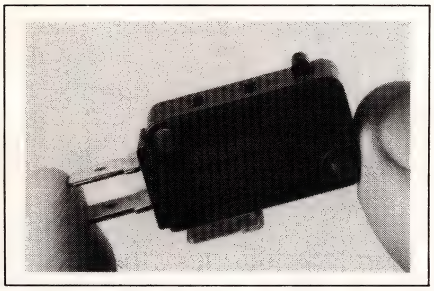
EDN 2587

The standard row spacing is 0.6 in., and leads are on 0.1-in. centers. The normally closed contact design minimizes pin stress and provides 100g of normal force per contact. When the cam is fully closed, the normal force increases by 50g per contact. This optional override position maintains electrical continuity even if the contacts are inadvertently damaged. A 24-position unit costs $3.39 (1000).

3M Corp, Box 2963, Austin, TX 78769. Phone (512) 834-6563.

Circle No 365



SNAP SWITCH

- *Actuation pressure of 200g*
- *UL listed and CSA approved*

This spdt snap switch measures 1×0.625-in. It is UL listed and CSA approved at 21A for 1 hp at 125V ac and 2 hp at 250V ac. The actuation pressure is 200g max. The switch features 0.25-in. quick-connect terminals, a fracture-resistant plastic body, and silver alloy contacts. It's available with a standard pin plunger or a variety of levers. $1 (OEM qty).

Pres:Air:Trol Corp, 1009 W Boston Post Rd, Mamaroneck, NY 10543. Phone (914) 698-2026.

Circle No 366

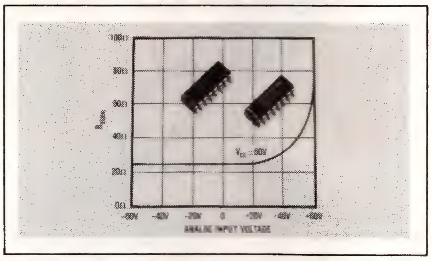
OPTICAL ATTENUATORS

- *5- to 30-dB loss increments*
- *Built with fusion techniques*

These single-mode and multimode fiber-optic attenuators are available with loss increments of 5, 10, 15, 20, or 30 dB, excluding connector losses. The loss tolerance equals ±0.5 dB. Standard attenuators are available with a variety of ½m-long bare-fiber pigtails. Cabled-fiber pigtails are available as an option. Built with fusion techniques, the attenuators are enclosed in a plastic cylinder measuring 0.19×2 in. $100.

Kaptron Inc, 3460 W Bayshore, Palo Alto, CA 94303. Phone (415) 493-8008. TLX 220883.

Circle No 367



ANALOG SWITCHES

- *Completely latch-up proof*
- *20-mW max operating power*

MAX 341 Series high-voltage CMOS/DMOS analog switches operate over a ±20 to ±50V supply range (20 to 60V with a single supply). The family includes dual-spst (MAX341 and MAX348), dual-spdt (MAX343), and dual-dpst (MAX345) switches. According to the manufacturer, the switches are completely latch-up proof, and they switch signals as high as the supply-rail voltages and introduce no offset voltages. The typical channel on-resistance specs at 80Ω for the MAX341/343/345 and 35Ω for the MAX348. All parts have a 20-mW operating spec and can be cascaded to switch as much as 0.5A. The switches feature make-before-break operation; they spec turn-on and turn-off times of 1 µsec max and 750 nsec max, respectively. All devices are available in versions for commercial, extended industrial, and military temperature ranges. $8.95 to $19.90 (100).

Maxim Integrated Products, 510 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 368

REAL TIME SERVICE

For five years, **MicroWay** has been the leader in 8087 support and accelerator board technology. People continue to buy our products for two reasons: one, they work and two, we support our products with one of the best technical support teams in the industry. Join those who know! Buy your 8087 support from **MicroWay.**

287TurboPLUS™
Speeds up your IBM AT!

An adjustable oscillator lets you increase your AT's 80286 speed in .5 MHz increments. Includes a 10 or 12 MHz 80287 clock and a system reset button.

Board only	$149
With 80287-10	$549
With 80287-12	$629
Optional 80286-10	$175

8087 Upgrades

8087	5 MHz	$114
8087-2	8 MHz	$149
80287-3	5 MHz	$179
80287-6	6 MHz	$199
80287-8	8 MHz	$259
80287-10	10 MHz	$395
NEC V20-8	8 MHz	$16
NEC V30-10	10 MHz	$30
64K RAM set	150 ns	$10
256K RAM set	150 ns	$27
256K RAM set	120 ns	$39
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CIRCLE NO 38

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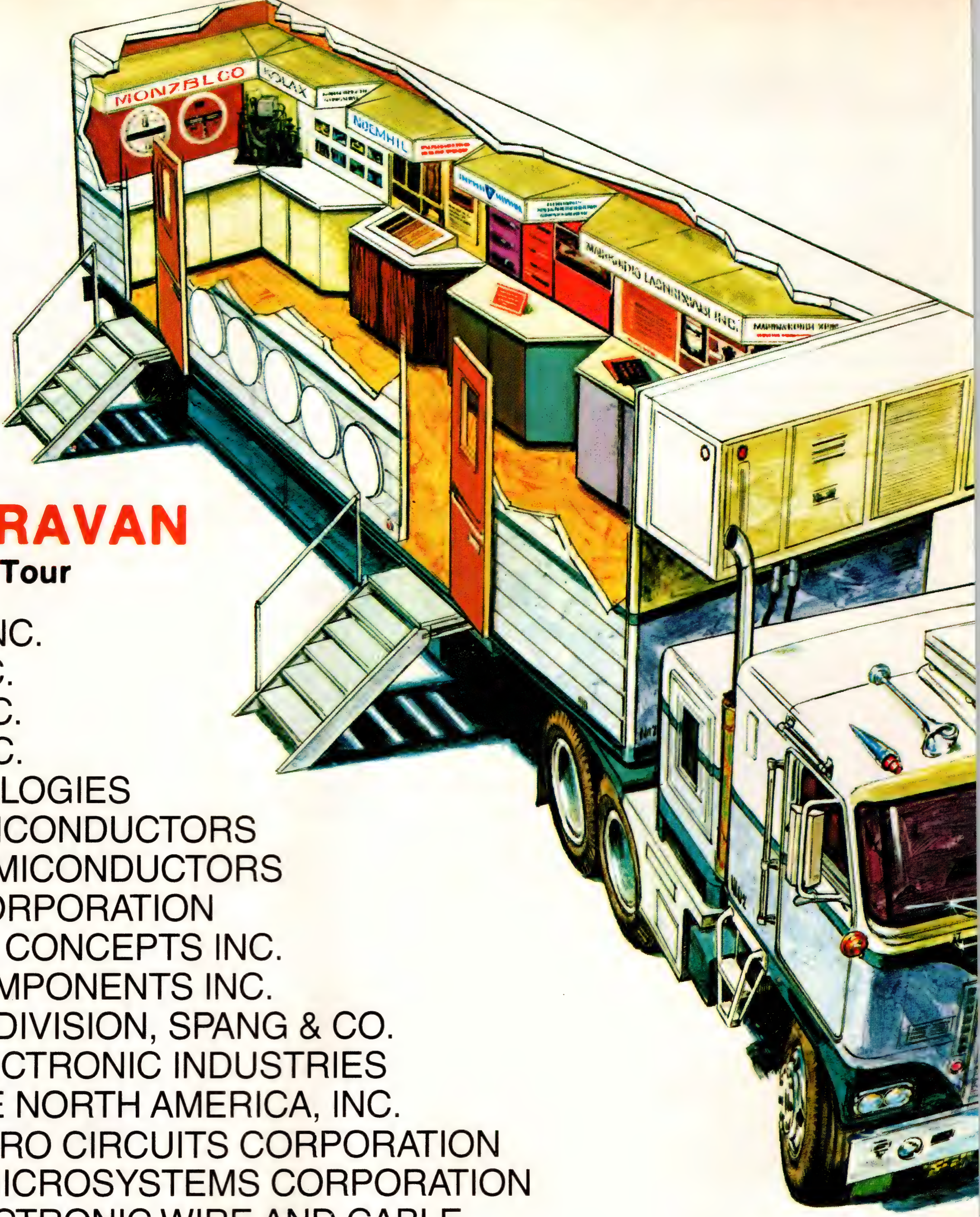

EDN CARAVAN

Western Show Tour

POWEREX, INC.
BOURNS, INC.
SOURIAU, INC.
GRAYHILL INC.
SFE TECHNOLOGIES
HARRIS SEMICONDUCTORS
PLESSEY SEMICONDUCTORS
LSI LOGIC CORPORATION
CONVERTER CONCEPTS INC.
STANTEL COMPONENTS INC.
MAGNETICS DIVISION, SPANG & CO.
TADIRAN ELECTRONIC INDUSTRIES
MURATA ERIE NORTH AMERICA, INC.
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STANDARD MICROSYSTEMS CORPORATION
BELDEN ELECTRONIC WIRE AND CABLE
GOULD INC., SEMICONDUCTOR DIVISION
CLIFTON PRECISION DIV., LITTON SYSTEMS, INC.
REXNORD SPECIALTY FASTENER DIVISION.

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1987 WESTERN EDN CARAVAN TRAVELING ELECTRONIC SHOW

February 9 to March 13 (first half)

DATE	TIME	SITE
2/9 Monday	9-12 AM	ROCKWELL INTERNATIONAL CORPORATION 3370 Miraloma Ave., Anaheim, CA
2/9 Monday	2-3:30 PM	NORTHROP CORPORATION 500 E. Orangethorp Ave., Anaheim, CA
2/10 Tuesday	9-12 AM	HUGHES AIRCRAFT COMPANY 1901 W. Molvern Ave., Fullerton, CA
2/10 Tuesday	2-4 PM	McDONNELL DOUGLAS CORPORATION 5301 Bolsa Ave., Huntington Beach, CA
2/11 Wednesday	8:30-10 AM	HUGHES AIRCRAFT COMPANY 2601 Campus Dr., Irvine, CA
2/11 Wednesday	11-1:30 AM-PM	FORD AEROSPACE & COMMUNICATIONS CORPORATION Ford Rd., Newport Beach, CA
2/11 Wednesday	3-4:30 PM	UNISYS CORPORATION 25725 Jeronimo Rd., Mission Viejo, CA
2/12 Thursday	8:30-10 AM	GENERAL DYNAMICS ELECTRONICS DIVISION 5011 Kearny Villa Rd., San Diego, CA
2/12 Thursday	10:30-12 AM	GENERAL DYNAMICS CONVAIR 5001 Kearny Villa Rd., San Diego, CA
2/12 Thursday	2-3:30 PM	TRW, INCORPORATED 15120 Innovation Dr., San Diego, CA
2/13 Friday	8:30-10 AM	HEWLETT-PACKARD COMPANY 16399 W. Bernardo Dr., San Diego, CA
2/13 Friday	10:30-12 AM	NCR CORPORATION 16550 W. Bernardo Dr., San Diego, CA
2/13 Friday	1-2:15 PM	M/A COM-LINKABIT INCORPORATED 3033 Science Park Rd., San Diego, CA
2/13 Friday	3-4:15 PM	M/A COM-LINKABIT INCORPORATED 10790 Roselle St., San Diego, CA
2/16 Monday	8:30-11:30 AM	LOCKHEED MISSILE & SPACE COMPANY 1111 Lockheed Way, Sunnyvale, CA
2/16 Monday	1-2 PM	FORD AEROSPACE & COMMUNICATIONS CORPORATION 1260 Crossman Ave., Sunnyvale, CA
2/16 Monday	2:45-4:30 PM	ESL INCORPORATED 495 Java Ave., Sunnyvale, CA
2/17 Tuesday	9-11 AM	HEWLETT-PACKARD COMPANY 5301 Stevens Creek Blvd., Santa Clara, CA
2/17 Tuesday	1-2:15 PM	APPLIED TECHNOLOGY 645 Almanor Ave., Sunnyvale, CA
2/17 Tuesday	3:15-4:30 PM	TANDEM COMPUTERS INCORPORATED 19333 Vallco Parkway, Cupertino, CA
2/18 Wednesday	9-11 AM	HEWLETT-PACKARD COMPANY 19447 Pruneridge Ave., Cupertino, CA
2/18 Wednesday	1-2:15 PM	APPLE COMPUTER INCORPORATED 20525 Mariani Ave., Cupertino, CA
2/18 Wednesday	3-4:30 PM	ROLM CORPORATION 4900 Old Ironsides Dr., Santa Clara, CA
2/19 Thursday	9-11 AM	HEWLETT-PACKARD COMPANY 1501 Page Mill Rd., Palo Alto, CA
2/19 Thursday	2-4 PM	GTE GOVERNMENT SYSTEMS 100 Ferguson Dr., Mountain View, CA
2/20 Friday	9-11:30 AM	FORD AEROSPACE & COMMUNICATIONS CORPORATION 3939 Fabian Way, Palo Alto, CA
2/20 Friday	1:30-3 PM	LOCKHEED MISSILE & SPACE COMPANY 3251 Hanover St., Palo Alto, CA
2/23 Monday	9-11 AM	HEWLETT-PACKARD COMPANY 1000 N. E. Circle Blvd., Corvallis, OR
2/23 Monday	2-4 PM	TEKTRONIX INCORPORATED Tektronix Industrial Park, Wilsonville, OR
2/24 Tuesday	9-11:30 AM	TEKTRONIX INCORPORATED Tektronix Industrial Park, Beaverton, OR
2/24 Tuesday	1-2:15 PM	FLOATING POINT SYSTEMS, INCORPORATED 3601 S. W. Murray Blvd., Beaverton, OR
2/24 Tuesday	3-4:30 PM	TEKTRONIX INCORPORATED Walker Rd., Beaverton, OR
2/25 Wednesday	9-11 AM	BOEING AEROSPACE COMPANY Space Center, Kent, WA
2/25 Wednesday	1-3 PM	BOEING AEROSPACE COMPANY 6811 204th So., Kent, WA
2/26 Thursday	9-11 AM	BOEING ELECTRONICS Lind Ave. & 39th St., Seattle, WA
2/26 Thursday	1:30-3 PM	HEWLETT-PACKARD COMPANY 8600 Soper Hill Rd., Everett, WA
2/27 Friday	8:30-10 AM	TEKTRONIX INCORPORATED Murdock Industrial Park, Camas, WA
2/27 Friday	10:30-11:30 AM	HEWLETT-PACKARD COMPANY 18110 S. E. 34th St., Camas, WA
2/27 Friday	1:30-3 PM	SURDSTRAND DATA CONTROL, INCORPORATED Overlake Industrial Park, Redmond, WA
3/2 Monday	8:30-10 AM	GRASS VALLEY GROUP INCORPORATED 13204 Bitney Springs Rd., Grass Valley, CA
3/2 Monday	1:30-3 PM	HEWLETT-PACKARD COMPANY 8000 Foothills Blvd., Roseville, CA
3/3 Tuesday	9-10:30 AM	HEWLETT-PACKARD COMPANY 1212 Valley House Dr., Rohnert Park, CA
3/4 Wednesday	9-11 AM	GM DELCO SYSTEMS OPERATIONS 6767 Hollister Ave., Goleta, CA
3/4 Wednesday	1-3 PM	RAYTHEON COMPANY 6380 Hollister Ave., Goleta, CA
3/5 Thursday	9-11 AM	HUGHES AIRCRAFT COMPANY 8433 Fallbrook Ave., Canoga Park, CA
3/5 Thursday	1-3:30 PM	LITTON GUIDANCE & CONTROL SYSTEMS 5500 Canoga Ave., Woodland Hills, CA
3/6 Friday	9-11 AM	LITTON DATA SYSTEMS 8000 Woodley St., Van Nuys, CA
3/6 Friday	1-3 PM	ITT GILFILLAN 7821 Orion Ave., Van Nuys, CA
3/9 Monday	9-11 AM	TELEDYNE SYSTEMS COMPANY 19601 Nordhoff St., Northridge, CA
3/9 Monday	1-3 PM	TELEDYNE ELECTRONICS 649 Lawrence Dr., Newburg Park, CA
3/10 Tuesday	9-12 AM	HUGHES AIRCRAFT COMPANY 2000 E. Imperial Way, Los Angeles, CA
3/10 Tuesday	2-4 PM	McDONNELL DOUGLAS CORPORATION 3855 Lakewood Blvd., Long Beach, CA
3/11 Wednesday	8:30-11:30 AM	HUGHES AIRCRAFT COMPANY 2000 El Segundo Blvd., El Segundo, CA
3/11 Wednesday	1-2:30 PM	XEROX CORPORATION 701 S. Aviation Blvd., El Segundo, CA
3/11 Wednesday	3-4:30 PM	NORTHROP ELECTRONICS 2301 W. 120th St., Hawthorne, CA
3/12 Thursday	8:30-10 AM	MAGNAVOX ADVANCED PRODUCTS & SYSTEMS COMPANY 2829 Maricopa St., Torrance, CA
3/12 Thursday	11-12 AM	GOULD INCORPORATED 4323 Arden Dr., El Monte, CA
3/12 Thursday	2-3:30 PM	HONEYWELL INCORPORATED 1200 E. San Bernardino, W. Covina, CA
3/13 Friday	9-11:30 AM	GENERAL DYNAMICS CORPORATION 1675 W. Mission, Pomona, CA
3/13 Friday	1-3 PM	AEROJET ELECTRO SYSTEMS 1100 W. Hollyvale, Azusa, CA

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Product	Part No.	Orgn.	Access Time (ns)	Packaging
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16K SRAM	HY61C16A	2Kx8	25,35,45,55,70	24-pin DIP (300/600)
16K SRAM	HY61C67	16Kx1	25,35,45,55,70	20-pin DIP (300)
16K SRAM	HY61C68	4Kx4	25,35,45,55,70	20-pin DIP (300)
16K SRAM	HY61C69	4Kx4	25,35,45,55,70	22-pin DIP (300)
64K SRAM	HY62C64	8Kx8	100,120,150	28-pin DIP (600)
64K SRAM	HY62C64A	8Kx8	35,45,55,70	28-pin DIP (600)
64K SRAM	HY62C87	64Kx1	35,45,55	22-pin DIP (300)
64K SRAM	HY62C88	16Kx4	35,45,55	22-pin DIP (300)
256K SRAM	HY62C256	32Kx8	55,70,90	28-pin DIP (600)

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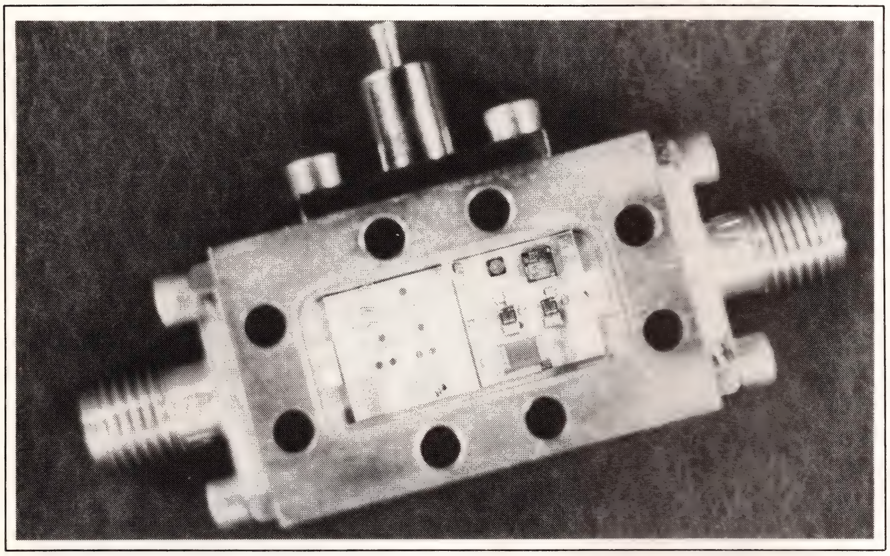
CIRCLE NO 129

NEW PRODUCTS

INTEGRATED CIRCUITS



GaAs MMICs

- *Includes low-noise, small-signal, medium-power amplifiers*
- *Spans the 2- to 6-GHz range*

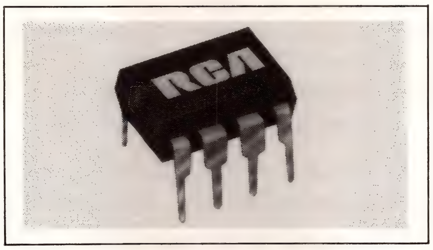
Housed in the manufacturer's miniature, removable-connector package (PMpac), this series of GaAsFET monolithic microwave amplifiers (MMICs) operates over the 2- to 6-GHz range. The family comprises low-noise, small-signal, and medium-power devices. Amplifiers having gain as high as 30 dB are available in the 1-in.-long housing. The low-noise series offers a 3.2-dB noise figure, a 10-dBm output power, and gain levels to 28 dB. For example, Model PM-CAM0601 has a 16-dB gain, a 3.2-dB noise figure, and a 10-dBm power output; the device draws 80 mA. The small-signal Model PM-CAM0615 specs a 24-dB gain, an 8.5-dB noise figure, and a 10-dBm power output, and it draws 110 mA. Medium-power units have power outputs to 18 dBm, gains of 16 to 31 dB, and noise figures as low as 3.5 dB. $700 to $1000.

Pacific Monolithics, 245 Santa Ana Ct, Sunnyvale, CA 94086. Phone (408) 732-8000.

Circle No 369

CLOCK CHIP

- *Drives quartz-controlled analog clocks*
- *Has output pins to drive stepping motor*



The Model CD22777 digital-clock IC is intended for time generation in quartz-controlled analog clocks. To generate its timing signals, the device requires an external 32.768-kHz crystal and a 30-pF trimming capacitor. Two motor-output pins in the device drive a clock's 1-Hz stepping motor; these pins each sink and source 3 mA min. The IC contains an alarm-output pin that generates a 2048-Hz pulse burst during each 32-sec period. Also included is a test-I/O pin that facilitates testing of the device. Housed in an 8-pin plastic DIP, the clock chip operates over −40 to +85°C from a 1.1 to 5V dc supply. The CD22777 draws a 5-µA max supply current. A version of the chip operates over −55 to +125°C. $0.41 (100).

GE/RCA Solid State, Box 2900, Somerville, NJ 08876. Phone (201) 685-6994.

Circle No 370

RS-232C CHIP

- *Contains line driver and line receiver*
- *Meets all RS-232C requirements*

This 1-chip RS-232C line-driver and -receiver IC incorporates the driver and receiver functions of the manufacturer's earlier SN75188 and SN75189A devices, respectively. The IC, Model SN75155, handles applications in which line lengths do not exceed 50 ft and data rates do not exceed 20,000 bps. The IC operates from dual supplies spanning ±4.5 to ±15V. It has a 10-mA, current-limited output and contains a 5V regulator. Response-control features include input-noise filtering and input-threshold shifting. Power-off output resistance for the TTL-compatible device is 300Ω typ. The 0 to 70°C chip is available in an 8-pin plastic DIP or an SO package. $0.73 (100).

Texas Instruments Inc, Semiconductor Group SC-658, Box 809066. Dallas, TX 75380. Phone (800) 232-3200.

Circle No 371

µP CHIP SET

- *Suitable for multitasking systems*
- *Includes µP, MMU, math chip*

The WE32200 chip set comprises the WE32200 µP, the WE32201 memory-management unit and data cache, and the WE32206 floating-point coprocessor. Suitable for multitasking systems, the chip set is

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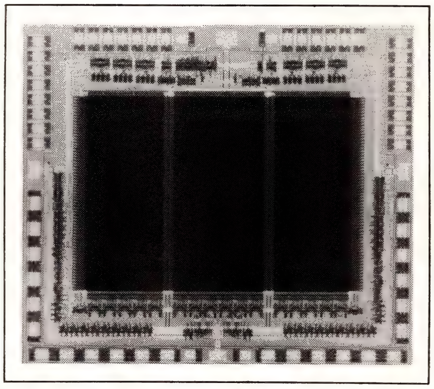
CIRCLE NO 41

initially available in a 24-MHz version. The WE32200 CPU, optimized for the Unix operating system, also accommodates other multiuser and multitasking systems. Model 32201 MMU has an on-chip, 4k-byte data cache that accommodates zero-wait-state virtual accesses at speeds as high as 30 MHz. You can connect as many as four 32201s together to provide 16k bytes of cache memory. The 32206 coprocessor can operate at speeds as high as 3.5M Whetstones/sec. Available software includes compilers for C, Fortran, Pascal, Basic, and Cobol, as well as math and I/O libraries, a symbolic debugger, assemblers, link editors, and disassemblers. WE32200, $500; WE32201, $550; WE32206, $425 (in quantities greater than 100).

AT&T Technology Systems, 555 Union Blvd, Dept KB, Allentown, PA 18103. Phone (800) 372-2447.

Circle No 372



DUAL-PORT RAM

- *Suits applications having multiplexed address/data bus*
- *Transfers data between systems having dissimilar word sizes*

The Model VT16AM8 dual-port RAM, intended for applications using a multiplexed address/data bus, can transfer data between systems having dissimilar word sizes. Like its earlier sibling, Model VT16DP8, the device's left port is organized as 1024 16-bit words and its right port is organized as 2048 8-bit words. The 16-bit port has a full address and data I/O field; you can configure the port to read and write in either word or byte mode. The 8-bit port multiplexes the eight low-order addresses with the eight data-I/O signals. The data access time is 60 nsec. The RAM incorporates all the interface logic required by 8- and 16-bit systems; it also contains contention-arbitration logic, an interrupt function, and automatic power-down for each port. In a 52-pin PLCC, $55.10 (1000).

VLSI Technology Inc, 1109 McKay Dr, San Jose, CA 95131. Phone (408) 434-3000. TLX 278807.

Circle No 373

STATIC RAM

- *Organized as 64k×1 bit*
- *Available with access times of 25, 35, or 45 nsec*

The HM65787 CMOS static RAM is available as a commercial-grade device (operating over 0 to 70 °C) with access times of 25, 35, or 45 nsec, or as a military-temperature-grade device (operating over −55 to +125°C) with access times of 35 or 45 nsec. In addition, it is available processed to MIL-STD-883C Class B requirements. All input and output data pins are separate and TTL compatible. Operating from one 5V supply, the RAM draws an operating supply current of 100 mA max and a standby current of 20 mA max. It's housed in a 22-pin plastic or ceramic DIP or in a chip carrier. A 35-nsec version in a plastic DIP costs $30 (100).

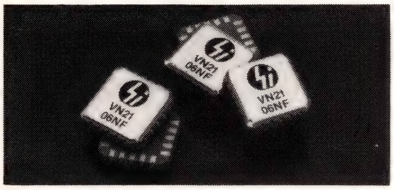
Matra-Harris Semiconducteurs, Les Quadrants, 3 avenue du Centre, 78182 Saint Quentin en Yvelines, France. Phone (1) 30438272. TLX 697317.

Circle No 374

Matra Design Semiconductor,

2840-100 San Thomas Expressway, Santa Clara, CA 95051. Phone (408) 986-9000.

Circle No 375



MOSFET ARRAYS

- *Available in surface-mount LCCs*
- *Contain four independent MOSFETs*

Models VN2106 NF and VN2110 NF arrays each contain four independent power MOSFETs in LCCs measuring 0.35×0.35×0.08 in. Specs for the two arrays include BV_{DSS} of 60 and 100V, respectively. For both devices, $R_{DS(ON)}$ is 3Ω max, C_{ISS} is 35 pF max, C_{RSS} is 15 pF max, and C_{DSS} is 5 pF max. The VN21 NF Series is available in commercial- and MIL-range versions and with MIL-STD-883 screening. For the MIL-temperature VN2106, $11.63 (1000).

Supertex Inc, 1225 Bordeaux Dr, Sunnyvale, CA 94088. Phone (408) 744-0100. TLX 6839143.

Circle No 376

GRAPHICS ICs

- *Combine TTL and ECL technology*
- *Operate from 250-MHz clock rates*

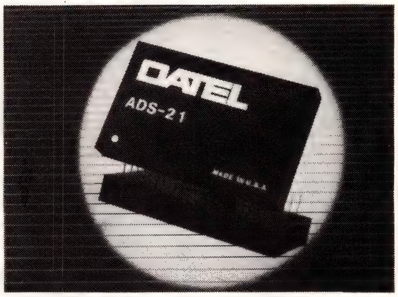
Two video-speed shift registers, Models 679501 and 679502, combine TTL and ECL technology. The devices operate at clock rates as high as 250 MHz. They incorporate 16 parallel TTL-compatible inputs and a serial ECL-10KH-compatible output. A transparent latch allows these cascadable devices to run in a pipelined configuration. The 679501 operates from one 5V supply; the 679502 uses a 5V supply for the TTL section and a −5.2V supply for the ECL section. The 679502 is pin compatible with AMD's Am8177. Both devices are targeted for graphics displays having resolution as high as 2048×2048 pixels. In 24-pin, single-width DIPs, 679501, $20.86; 679502, 16.68 (100).

Monolithic Memories Inc, 2175 Mission College Blvd, Santa Clara, CA 95054. Phone (408) 970-9700. TWX 910-338-2376.

Circle No 377

A/D CONVERTER

- *Provides 12 bits at 1.3 MHz*
- *Uses thick- and thin-film technology*



Combining a 12-bit A/D converter and a track/hold amplifier in one package, Model ADS-21 sampling A/D converter provides 12-bit resolution at a 1.3-MHz sampling rate. The converter achieves its speed through the use of a digital subranging architecture. It contains hermetically sealed hybrids in a 46-pin DIP capable of operation over 0 to 70°C, and it dissipates 2.4W max from ±15 and ±5V supplies. $565 (100). Delivery, stock to eight weeks ARO.

GE Datel, 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-9341. TWX 710-346-1953.

Circle No 378

Program ALL Your PLDs for ONLY $2495.

The ELAN MODEL 1011 Programs Virtually ALL PALs, CMOS PALs, FPLAs, and EPLDs with unmatched features for ease-of-use:

- Automatically displays equivalent devices - No clumsy wall charts needed!
- English language prompts on easy-to-read display take you step-by-step through all tasks.
- Operates stand-alone or under control of computer or development system.

Detailed Feature Summary

- 64K byte user RAM standard (expandable to 512K bytes)
- Built-in diagnostics assure reliable performance
- Device update via easily replaceable cartridge
- Certified by Semiconductor Manufacturers
- Devices protected against improper insertion

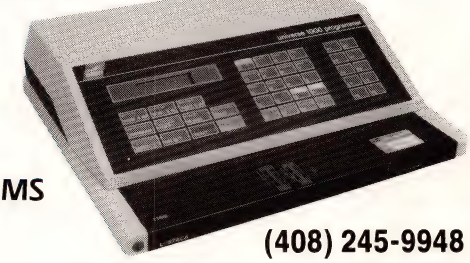
Also Available:
Model 1012 BIPOLAR & EPROM Programmers at $3495.

elan

ELAN DIGITAL SYSTEMS
720 N. Fairoaks Ave., #91
Sunnyvale, CA 94086

(408) 245-9948

CIRCLE NO 39



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EDN Product News

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

INSIDE

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- 3 DIP switch
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- 1 Enclosures
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TECHNOLOGY UPDATE

Enclosure makers respond to system-packaging needs

Donna Coco,
Assistant Editor

technologies dictate system-packaging requirements, however, manufacturers respond with appropriate products.

has resulted in enclosures that meet demands for increased strength, as more equipment is squeezed into smaller spaces. Manufacturers have also responded to demands for enclosures that are easy to use; current products have fewer parts and provide access without disassembly. Many offerings combine design versatility with off-the-shelf promptness.

continued on page 15

TECHNOLOGY UPDATE

CMOS the choice for multiplying D/A converters

Tammi Harbert,
Staff Editor

Recent product introductions illustrate that CMOS has become the technology of choice for multiplying D/A converters (DACs). Demand for the process' low cost, low power dissipation, and its capability to allow 4-

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A CAHNERS PUBLICATION

EDN CareerNews

For Engineers' Professional Growth and Development

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First Seminar Service 1
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CareerCALENDAR 2

Seminar Service Helps EEs Cope With Technology Explosion

By Michelle Cody

Keeping abreast of the newest developments in technology is vital to an engineer's ability to survive in an increasingly competitive job market. Studies on the erosion of technical knowledge show that technical skill, particularly among engineers, becomes obsolete within five years. Ironically, two of the factors that contribute to that erosion—specialization and rapid technological advancement—characterize the high-tech industry.

First Seminar Service helps engineers find the appropriate seminars, conferences, and courses to keep them technically astute. The service's database contains thousands of engineering seminars run by some of the most familiar education sources in the electrical engineering profession, including Worcester Polytechnic Institute, the Software Institute of America, the Institute for Advanced Technology, and the Center for Professional Development.

Knowledge Network

Founded by John Tumminello, a former Prime Computer training director, First Seminar Service has been in full operation for about one year. According to Tumminello, the service was created to serve as a network through which professionals could satisfy their continuing need for new knowledge. "An engineer's lifeblood is to know what the next best thing will be," he says. "But everything is constantly changing. How does an engineer keep up?"

Riding the Fast-Growth Express

By Kate Colborn

Engineers who work for fast-growing companies face considerable pressure, but many say the rewards are worth it.

"The biggest thrill is to be the only engineer on a project," says Scott McMorrow, manager of memory marketing and applications for Lattice Semiconductor in Beaverton, Ore. "I can't describe the high when you see the results of your efforts," says Laurie Lauchlan, senior development engineer with Integrated Device Technologies, a semiconductor manufacturer in Santa Clara, Calif. These sentiments are echoed by engineers in a variety of companies. For hardware and software people, managers and recently-hired graduates, interesting, responsible work is the first prerequisite for a good job — well ahead of salary level or benefits.

One of the most likely places to find a job that offers autonomy and stimulation is with a company whose engineering staff is growing rapidly. "If the company is growing, the people are growing," observes Mark Jarvis, product design engineer for Ford Motor Company's Electrical and Electronic Division in Dearborn, Mich.

Startup electronics companies are the most obvious place to find rapid, sometimes mind-boggling growth, but companies of all sizes and in all stages of development expand their engineering workforces in response to business demands and company policies. Even within giants like Northrop Corp., E-Systems, and Ford Motor Company, divisions and operating groups are adding staff at a rate that has a major impact on the jobs of their engineers. *Career News* talked to engineers in a dozen companies about how engineering staff growth has affected their jobs. The responses reveal several common observations and concerns.

Opportunities To Grow

Growing companies offer plentiful opportunities to do interesting work, expand technical and managerial skills, and

Engineers' Satisfaction a Key to Company Success

By
Marjorie Stenzler-Centonze

Motivating engineers is vital for the health of any high-tech organization. Companies are finding more creative ways to attract and hold on to valuable EEs.

Top companies in the electronics industry cite engineering talent as the key factor in maintaining their competitive edge. Says Roger Brown, vice president of industrial relations at Sanders Associates of Nashua, N.H., "The developments that come out of a progressive and innovative engineering department determine a company's ability to stay competitive in the marketplace." At Burroughs Corp., Detroit, Mich., director of employment Howard Owens concurs. Although Owens believes marketing to be important, he sees top engineering talent as absolutely critical to company growth. "Product cycle times are shortening, and there's tremendous pressure on product improvement both in hardware and software development," Owens states.

Regardless of size or age, all electronics companies must find ways to attract high-quality engineers and motivate and maintain them once they are on board.

Creative Work Environment

Assuming that salary and benefits packages are competitive, one of the most attractive qualities a company can boast is a creative work environment that allows and encourages engineers to take risks. Such an

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A QUICK LOOK

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Priam signs OEM contracts with four companies for $18.5M of disk-drive business. Page 3

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Research engineers at the University of Illinois have developed a plasma display panel that uses half the circuits normally required. Page 3

MIL Standards
GE/Intersil, Maxim qualify products for MIL-STD 883B, Rev C. Page 5

Custom Software
Genesis Microsystems has entered an OEM agreement to provide ZAX Corp. with its custom debugging software. Page 9

Design Center
Minnesota-based VTC Inc. opens its first remote design center in San Jose, CA. Page 9

Price Cuts
Touch-terminal maker Electro Mechanical Systems drops prices by as much as 40%. Alter drops EPLD prices by 36%. Page 13

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PRODUCTS

DSP Board Fits IBM PC

The EVK-128 provides signal-processing hardware and FIR-filter design and modification software. You can copy all or part of the system for use in your own signal processor.

GE/Intersil's EVK-128 combines A/D conversion and FIR filtering

JEFF HAIGHT
GE/Intersil Inc.

As digital signal processing becomes simpler, cheaper, and more pervasive, the boundaries between design ideas and design techniques must give way for a more integrated approach to system development. Intersil's EVK-128 board, which occupies one slot in an IBM PC, incorporates analog design and digital signal-processing techniques.

The board works in such applications as PC-based analog or digital data-acquisition and digital filtering systems, finite-impulse-response (FIR) filter design and development systems, or as part of an FIR filter processor for off-line or non-real-time data.

The system (**Fig. 1**, below) offers an active antialiasing filter, power-supply circuitry, A/D and D/A converters, and digital interfacing and control circuitry. The board also has FIR filtering circuitry and software for FIR design, modification, plotting, and control. Documentation includes itemized parts lists, schematics, timing

continued on page 19

TECHNOLOGY

Power MOSFET Makers Boost Electrical Specs

Manufacturers improve electrical characteristics and offer a host of package types

TAMMI HARBERT
Staff Editor

Recent power-MOSFET introductions offer lower on-resistance, higher voltage, faster switching, and innovations in onboard intelligence. Packaging improvements include greater electrical isolation and an increased availability of plastic and surface-mount parts.

Among the manufacturers of low-on-resistance devices are some companies well known in the power-MOSFET industry: Siliconix, Fairchild, International rectifier, and General Instrument. Newer manufacturers—IXYS, for example, have also entered the arena.

Low-on-resistance parts

Made for applications requiring low on-resistance, Siliconix's SMM70N05 is built using the company's MOSPower-6 technology, which produces a chip density of 1.6M transistors/in². The device has an 18-mΩ on-resistance with a continuous current rating of 70A. The 50V SMM70N05, a follow-on to the company's SMP60N05 and SMM60N05, is available in TO-3 packaging for $10.11 (1000).

Like the SMM70N05, the SMP- and SMM60N05 are 50V MOSPower-6 devices. Unlike the newer device, however, these parts offer current and on-resistance of 60A and 23 mΩ respectively. Another de-

continued on page 21

CAREERS

The Temptations of Temping

Once confined to the clerical realm, temping grows in popularity among EEs.

RUTH CLOGSTON

Chris Clark, a 30-year-old programming consultant from Hopkinton, MA, has worked as a contractor for six months. He started temping because he wanted freedom and independence—he is developing his own software and needs to avoid the conflicts of interest

continued on page 58

COMPANIES WITH EXPANDED OPTIONS

EEs are increasingly being drawn toward temping

In January, EDN Product News and EDN Career News, EDN's two tabloid editions, merge to form EDN News... bringing you all the hottest news of products, technology, and careers.

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The focus of EDN News is on hot products that will have the most powerful impact on the way you do your job. EDN News will cover the best products on the market, how they evolved, and why. Plus, it will now cover industry events (news of business, finance, economics) that drive product technology and hence product introductions.

HOT NEWS OF CAREERS

In a separate section, EDN News will keep you abreast of professional developments and job openings in the electronics field. It will carry editorial aimed at your career and professional growth. Editorial that will help you find a job and keep it.

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CIRCLE NO 130

NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

STD BUS DEVELOPMENT

- *Has hardware and software development facilities*
- *Uses IBM PC for control, display, and file storage*

The LM-1 linker module is an STD Bus board that plugs into a slot of a target system and acts as an I/O-mapped slave for the STD Bus's CPU. The board has two serial RS-232C ports for communicating with an IBM PC or compatible and for downloading programs to serial EPROM programmers. A parallel printer port features Centronics-style handshaking. You can develop programs on your IBM PC and download them to the STD Bus target system via the linker for debugging. Versions are available for Z80, 8085, and 8086/88 target systems. Software supplied includes Linker software for the PC, which links the PC and the target system, and debugging software. In addition, some debugging firmware in an EPROM is located on the linker board but is resident in the STD Bus memory-address space. As an option, the vendor can supply SL/M, a compiled language that's similar to Basic and designed for program development. SL/M is optimized for systems that are rich in parallel I/O interfaces. LM-1 hardware with Linker software and firmware, $695.

Devtek Systems, Box 5224, Lancaster, PA 17601. Phone (717) 560-0652.

Circle No 379

DSP DEVELOPMENT

- *Lets you develop DSP programs on an IBM PC or compatible*
- *Provides a TMS32010 processor and an analog subsystem*

The DSP-320 development system consists of three components: the vendor's DSP-D digital board, which loads and runs programs on the Texas Instruments TMS32010 digital signal processor; the DSP-A analog board, which provides A/D and D/A peripheral interfaces for the TMS32010 processor; and the vendor's ASM-10 assembler, which lets you develop TMS32010 programs on an IBM PC or compatible and then download them to the DSP-D board for execution. The DSP-D board consists of a TMS32010 running at 20 MHz; an 8039 μC for local control of the TMS32010 and RAM; as many as 4k bytes of RAM for program storage; and ROM-resident firmware for communication with a video terminal or with an IBM PC via an RS-232C serial port. The firmware also allows you to use a tape recorder to store and load programs. Using the 40-pin header included in the package, you can connect the DSP-A analog subsystem, which provides 8-bit A/D and D/A converters, jumper-selectable sampling-clock rates as high as 20 kHz, and analog filters for antialiasing and reconstruction of analog signals. Written in C, the assembler runs on an IBM PC or compatible. It accepts standard TI mnemonics and generates executable object files that you can download directly to the DSP-D board. The vendor also offers power supplies and a 60-pg manual of experiments. DSP-D board, $299; DSP-A board, $199; ASM-10 assembler, $129.

Microcraft Corp, Box 513, Thiensville, WI 53092. Phone (414) 241-8144.

Circle No 380

8051 μC DEBUGGER

- *Has 8051 assembler in firmware*
- *Provides emulation and debugging facilities*

The SDS-8051 lets you develop and debug software to run on an embedded 8051 μC. The unit contains an 8051 assembler program in firmware, so that you can develop assembly-language programs on your target machine. A bond-out 8051 μP, which has extra nodes that give you access to internal signals, provides real-time emulation facilities; it allows you to set and monitor the CPU registers and keep control of the program currently running. The unit has two RS-232C serial ports; you can use one of these ports to connect a console terminal and the other to link the debugger to an IBM PC. You can then download application programs developed on the PC with the aid of a cross-assembler. Alternatively, you can use an IBM PC or compatible, running in dumb-terminal mode, as the console. If you're developing software for a target machine that doesn't yet exist, you can use the simulation mode of the debugger to run and debug the software. $5495.

Phillips & Signetics Micro-Systems Inc, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-3595.

Circle No 381

Phillips, Industrial & Electroacoustical Systems Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone 040-757005. TLX 51573.

Circle No 382

IMAGE PROCESSING

- *Lets you create graphics and text*
- *Provides extensive image-processing and analysis functions*

DT/Image-Pro is a real-time image-processing software package that runs on the IBM PC/AT and compatibles equipped with the vendor's DT2851 frame-grabber board and optional (but recommended) DT2858 auxiliary frame-processor board. The software lets you label images; add grids, lines, or ellipses to them; and paint over or cut and paste portions of images. Using a mouse, you select the operations from a hierarchy of menus. The main menu offers major function categories such as image analysis, image measurement, and image editing with the aid of the built-in graphics editor. Submenus offer acquisition, processing, and display functions. The filters provided include lowpass, highpass, Laplacian, horizontal-edge, and vertical-edge enhancement; a special editor lets you create custom filters. You can shrink images to fit a window, magnify them for closeup examination, or rotate them interactively to a particular angle. You can also generate histograms that display the frequency distribution of gray levels in line, windows, or whole images. The package includes the Halovision graphics editor that allows you to create graphics and text and mix them with acquired images. DT/Image-Pro, $1495; DT2851 frame-grabber board, $2995; DT2858 frame-processor board, $1695.

Data Translation Inc, 100 Locke Dr, Marlboro, MA 01752. Phone (617) 481-3700.

Circle No 391

CAD SYSTEM

- *Can import and export drawing files in ASCII and IGES*
- *Produces drawings with 0.005-in. resolution*

Prodesign II runs on the IBM PC and compatibles and works with most printers and plotters available for the IBM PC, as well as with a wide variety of graphics adapter cards, digitizers, and mice. The virtual-screen feature lets you generate graphics from your standard graphics adapter and monitor, but also works with the IBM Enhanced Graphics Adapter and other high-resolution-display units. The hard-copy output features let you generate plotter-quality drawings on a standard dot-matrix printer. You can operate in command mode or from menus, and you can use a mouse or digitizer. It lets you move, copy, erase, or save any part of your drawing; an undo command cancels the effect of your last command. The program provides 16 colors, and a drawing can have as many as 30,000 points. You can create as many overlays as you wish in the design of multilayer boards, and you can create isometric views of a section. The program imports any H-P plotter file and ASCII files of X-Y coordinates, and it imports and exports data files that conform to the International Graphics Exchange Standard. It requires IBM Color Graphics Adapter or equivalent, 512k bytes of RAM, and two 360k-byte floppy-disk drives or a hard-disk drive. $299.

American Small Business Computers Inc, 118 South Mill St, Pryor, OK 74361. Phone (918) 825-4844.

Circle No 392

GATE-ARRAY CAD

- *Runs on IBM PC, PC/XT, or PC/AT*
- *Includes a PLD conversion package*

Running on an IBM PC, PC/XT, PC/AT, or compatible computer with 640k bytes of memory and an EGA board and monitor, the Gate Aid Plus/PC software allows you to use the company's MA Series of 3-μm, single-layer-metal gate arrays. The software includes schematic-capture, gate-level simulation, testability-analysis, and fault-simulation capabilities. It also includes a PLD converter package that allows you to integrate several programmable-logic arrays into one ASIC. Enhancements to the software, which will allow you to design with the company's MB Series of 2-μm, double-layer-metal gate arrays, are under development. Less than $15,000.

Matra-Harris Semiconducteurs, Les Quadrants, 3 avenue du Centre, 78182 Saint Quentin en Yvelines, France. Phone (1) 30438272. TLX 697317.

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Matra Design Semiconductor, 2840-100 San Thomas Expressway, Santa Clara, CA 95051. Phone (408) 986-9000.

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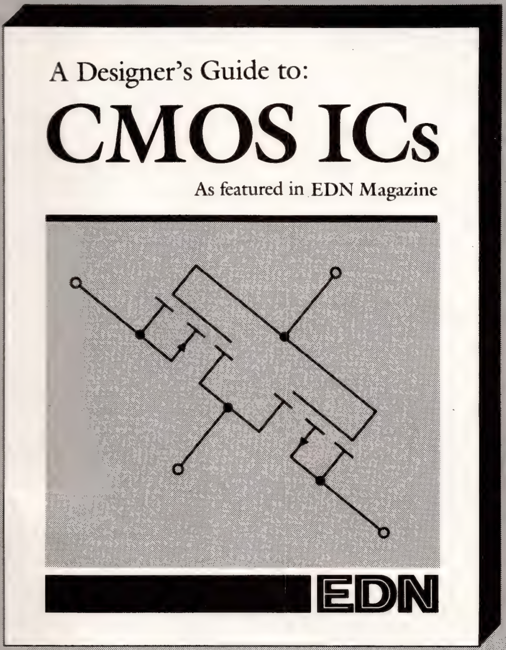
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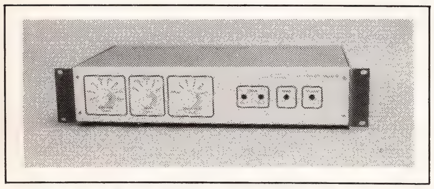
STS Instrument Corp, 6114 La Salle Ave, Suite 329, Oakland, CA 94611. Phone (415) 339-3264.

Circle No 383



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The SX/11 satellite data-link simulator simulates the two major degrading effects on digital transmission via satellite: delay and random errors. It can either simulate an entire full-duplex data link or add errors and delay to an existing link. The unit operates at all standard rates between 2.4k and 64k bps. You inject delays of between 0 and 1.0 sec with 0.25-sec resolution. The unit also injects pseudorandom bit errors at error rates between 0 and 10^{-7}. Both data streams experience the same error rate, although the errors are uncorrelated. The SX/11 can come with RS-232C, V.35, or RS-422 modular interfaces. $2670 to $2790.

Adtech Inc, 1814 Algaroba St, Honolulu, HI 96816. Phone (808) 941-0708.

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Mini Tool Inc, 1334/F Dell Ave, Campbell, CA 95008. Phone (408) 374-1585.

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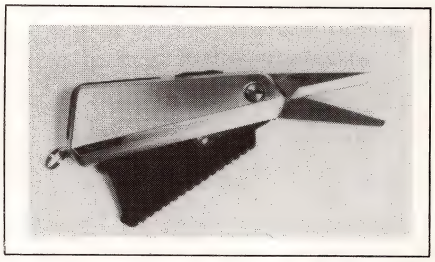

BOARD FABRICATOR

- *Has CAD interface*
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The Protoflex-III Model PF-IIIA prepares prototype pc boards without using chemicals. It can work from either prepared artwork (including magazine illustrations, positives, or negatives) or a file downloaded from a computer. The device machines circuit boards at 75 in^2/hour from 1-oz, tin-plated copper sheeting on a thin polyimide base. You subsequently glue the thin material to a regular pc-board base. $19,300. Delivery, 8 to 12 weeks ARO.

Girard Electronics, 13914 W Oakgreen Circle S, Afton, MN 55001. Phone (612) 436-1167.

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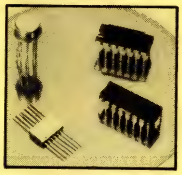

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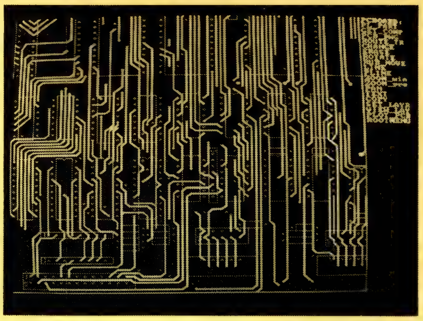

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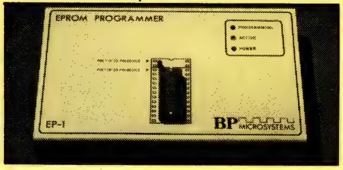

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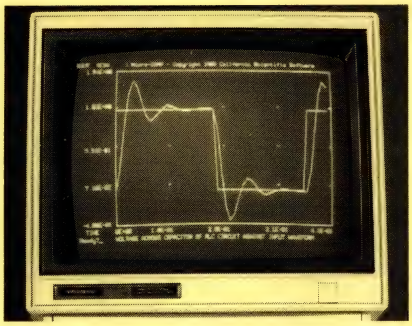

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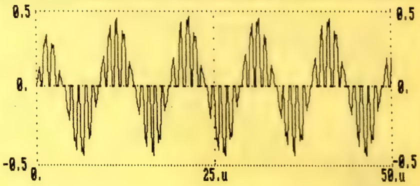

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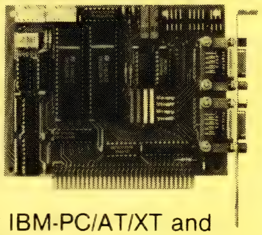

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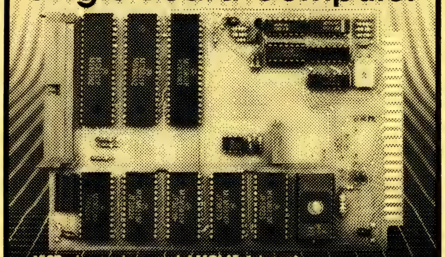

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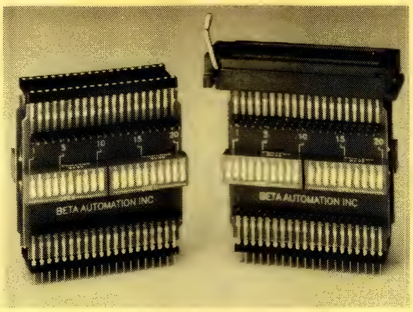

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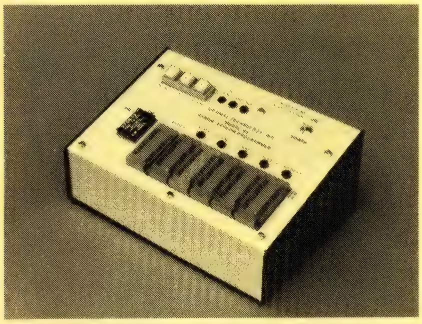

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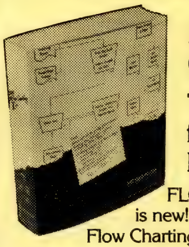

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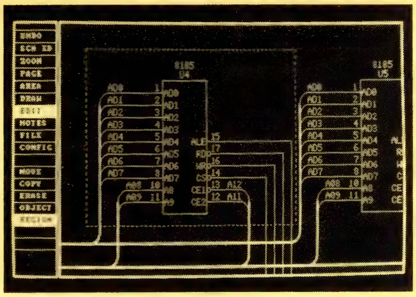

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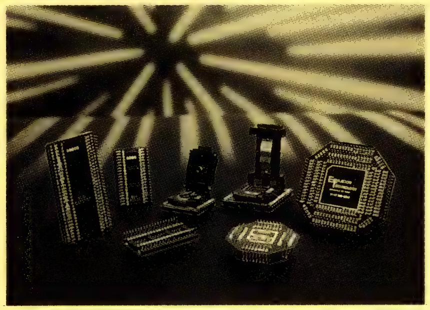

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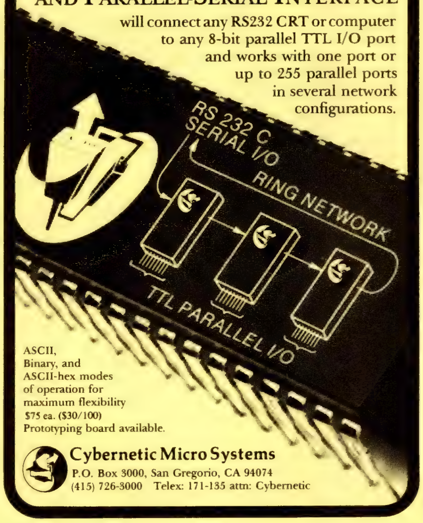

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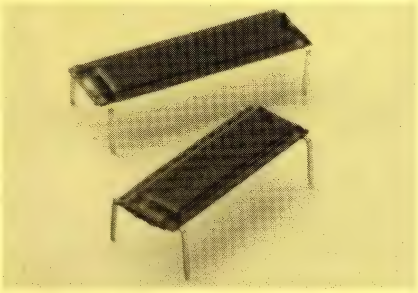

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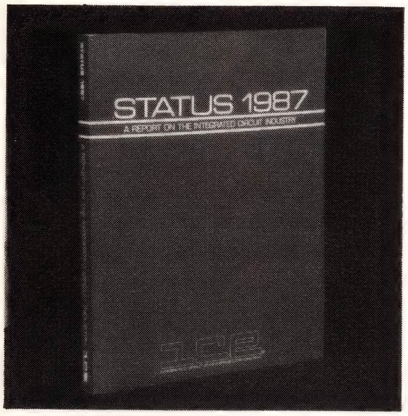

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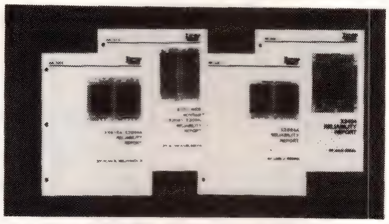

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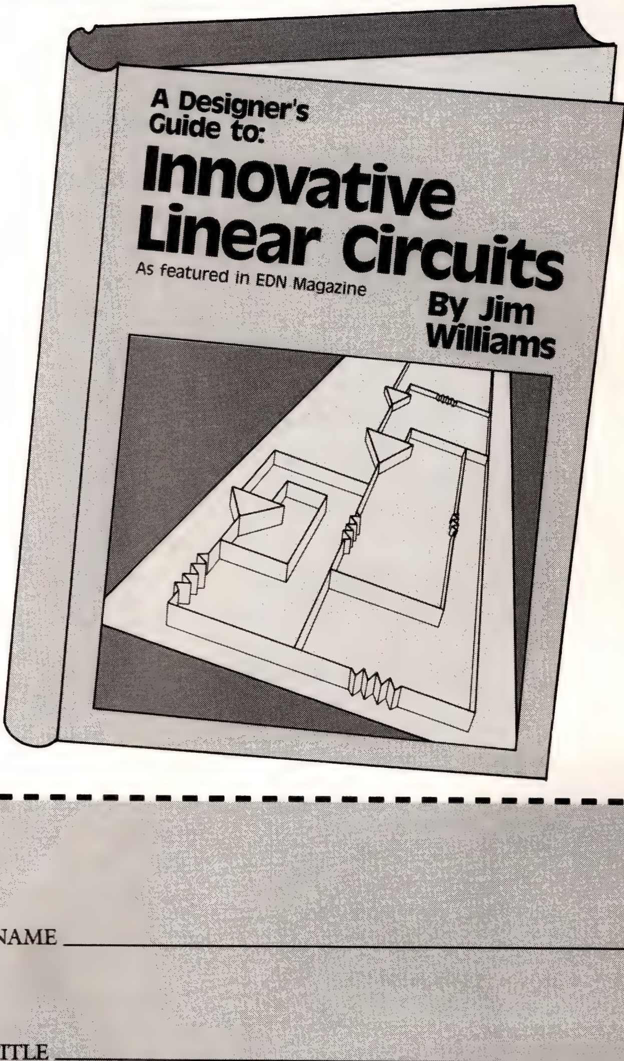

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Jim Williams: Circuits as art

Deborah Asbrand, *Associate Editor*

After spending years on the design of a particular group of circuits, analog-circuit designer Jim Williams sat down at his laboratory bench only to discover that the system didn't work. Months of refinement still could not get the circuits to do their intended job, which was to measure the small amounts of heat produced in a biochemical reaction. After yet another application of the soldering iron, a trace on the oscilloscope began to oscillate very slowly and then settled to a dc value. The circuits were working.

"I went crazy, running down the hall and out onto the grass," remembers Williams, who was then teaching and conducting research at MIT. "I ran into Walker dining hall and I yelled, 'It worked!' I had a one-man celebration and ran all over the campus."

Williams's enthusiasm that day is typical of the zeal that has marked his successful if unorthodox career in electronic engineering. Although his only college education consisted of the year and a half he spent studying psychology at Wayne State University, he began teaching electronic circuitry at MIT at the age of 20. Since then, he has devoted himself to analog-circuit design. In recent years, his career has taken a new turn: Now working for Linear Technology (Milpitas, CA), he spends a good portion of his time writing analog-circuit applications articles for electronics trade magazines.

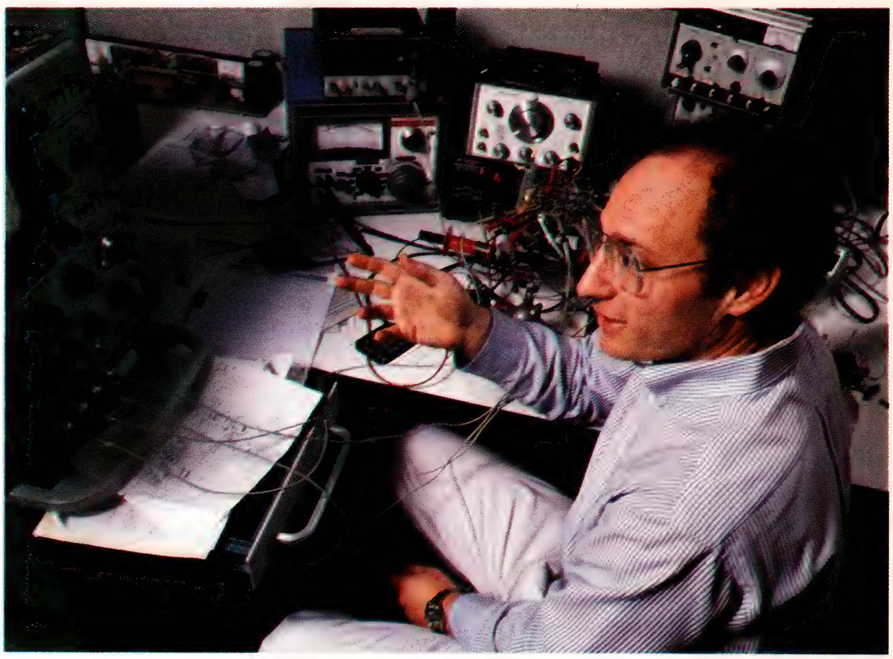
Williams's approach to his work is equally unconventional. For him, designing circuits is not work at all, but an artistic endeavor that is—above all—fun. The circuit-as-art theme is evident in Williams's office, where mounted on the wall behind his desk is a colorful painting of a high-voltage amplifier circuit. Six circuit boards from the Minuteman missile-guidance system sit on top of his desk, creating a rainbow with their colorful protective coatings. Also on his desk is a package addressed to "Dr Jim Williams," the sender unaware of Williams's brief student career.

In fact, aside from the 10 years he spent as an instructor at MIT, the most fertile educational ground for Williams proved to be television-repair shops. Growing up in Detroit, he rummaged through the dumpsters behind repair shops, plucking out discarded circuit boards and lugging them home to pull apart. At 14, he got a job repairing televisions. And in 1968, when he decided to drop out of college and move to Cambridge, MA, to be closer to MIT's technical community, he supported himself by working as a TV repairman.

When Williams arrived in Cambridge at the age of 20, he had no classroom training in engineering. In fact, he had developed an acute aversion to the rigid structure found in most classrooms. But he did like to learn, and he brought to Cambridge a wealth of knowledge culled from years of dissecting shortwave radios, fans, and heaters: years of "bumbling around circuits," as he calls it. He started hanging around

Photographs by Tim Davis

the MIT campus and eventually met a professor who got him a job as a technician in a campus laboratory.



A pivotal friendship

Among the bonds he established early during the MIT years was his friendship with the late Jerrold Zacharias, a professor emeritus of physics and an internationally recognized nuclear physicist. Leader of the engineering division of the Manhattan Project, Zacharias had taught at MIT for 30 years. His research on the radio-frequency spectra of atoms led to the development of the first atomic clock.

Believing that the conventional education system discriminated against individuals who didn't fit within its narrow confines, Zacharias actively worked for educational reform. He was instrumental in the formation of the Physical Sciences Study Committee, a group whose revamped curriculum for teaching high-school physics is now widely used.

Learning through teaching

After being introduced, Williams and Zacharias talked at length and often "about everything from Archimedes to art to physics to biochemistry to education to circuits," Williams says. "One day he said to me, 'If you don't like to learn [in a classroom], maybe you'd like to teach.' Zacharias said the best way to learn is to teach."

"Digital didn't seem to have any charm or poetry. I could see where it would be challenging and difficult, but it always seemed that analog design was much prettier."

With Zacharias's support, Williams began teaching electronic circuitry to MIT students, and he thrived on teaching to others what he had learned on his own. In fact, classroom learning took on a new look for him. "I loved it. In that role, I enjoyed going to school," he says. "For tests, I'd give students problems to work on and tell them they could talk to me or to other people in class or they could use the library. A final exam was three or four weeks long.

"I wasn't interested in whether they got the right answer—I was interested in how they approached the problem, how they perceived it, and how they pursued it. I thought that was more useful intellectually. I'm sure Einstein was able to look up anything in the library when he was pursuing the theory of relativity."

Analog's allure

Comfortable in the academically open atmosphere at MIT, Williams continued to teach there for the next nine years. And his love of analog-circuit design grew steadily throughout that period. In spite of the phenomenal growth in digital design at that time, he remained fascinated by the intricacies of linear circuits. "Digital didn't seem to have any charm or poetry," he says. "I could see where it would be challenging and difficult, but it always seemed that analog design was much prettier."

Indeed, linear design's great appeal for Williams is aesthetic, and his conviction that designing is an art goes far beyond decorating his office with circuit boards. "I don't see any difference between a breadboard and a sculpture, and I never have. A circuit is a piece of sculpture because it's got a physical form —colors, shapes, lines—soul and emotion."

Williams looks at circuit designs much the same way some people approach a painting or a sculpture. "You look at it and wonder why did the designer decide to do it that way, what is his history, who did he work with? What are the hidden motivators? I can look at a circuit and know 'That's Paul Brokaw of Analog Devices.'"

An aficionado of the visual arts, Williams includes among his favorite artists sculptor Alexander Calder, known for his deft juggling of form and space, and painter Joan Miro, a modernist whose paintings are noted for their humor and gaiety. Williams's designs express a combination of those qualities: Working in the three-dimensional medium of circuit design, he is more artist than engineer, yet despite his obvious zeal for his work, he maintains a lightness and irreverence about what he does, interspersing his artistic analogies with confessions that his job is mostly "horsing around."

While working on a particular project, Williams focuses all his energy on the design itself. "Things that are completely disparate remind me of a piece of the circuit," he says. "The way food is arranged on a plate, for example. If you go to hear the symphony, you hear the way the horns and the strings blend together, and you think, 'That's the way the base and emitter current come together.' You're lovesick for the circuit."

So personal an expression are Williams's circuits to him that they form a picture book of his life. Looking at one of his designs, he can intuit what was happening in his life at the time. "During the times when I was happiest emotionally, the circuits are simple, minimal, direct, more closely approaching elegance. At times when I was less happy, there is a lot of clutter."

Technological intrusions into the analog artist's world don't faze Williams. Despite the innovations of analog CAE techniques, linear circuits remain best designed first on paper and then manually on a breadboard, he says. "Much of the ultimate achievable perfection is defined by the imperfection of the components and the skills of the designer in getting around that." He happily remains "virtually digitally illiterate. I've never programmed a computer or designed a digital circuit. I can't give you the truth tables for simple logic gates."

As for his analog-design skills, he says they reflect "lots of enthusiasm and not too much formality." An abundance of impatience makes him "more likely to try something than to think about it," he says. "I iterate rather than create. I've seen people who can pull elegantly simple ideas out of their heads, but I have to slosh through the mud to get where I'm going."

"Some people think about skiing while they're at work; I think about circuit design while I'm skiing."

By his own definition, his analog chauvinism precludes his presence among the elite designers. "The best circuit designers I've seen are generalists . . . . They don't view themselves as analog designers or digital designers. They look at themselves as working within the whole spectrum of design and they use whatever tool is required."

At age 38, Williams has already achieved a goal that is high on many people's lists: He is doing what he loves to do. He became an independent consultant after leaving MIT in 1978, and then worked as a linear designer for National Semiconductor. In 1981, he became a staff scientist at Linear Technology; it's the company's highest ranking title for nonmanagers.

At Linear Technology, Williams spends one half of his time on applications designs and the other half writing articles on analog design. The decision to devote such a large chunk of his time to writing is part mission—to spread the analog gospel—and part career move. Too many engineers, he says, leave their careers to the vagaries of fate and the economy. Writing articles is a way for Williams to sharpen his writing skills and enhance his marketability.

In his present job, Williams also participates in policy-making decisions, a responsibility he says irks him when he has to drop a design project to attend executive meetings, yet also serves to relieve him of his "white-socks laboratory existence." Like other designers at the company, he works informally with a young engineer, teaching him the finer points of analog circuitry and acting as a mentor, a role he consid-

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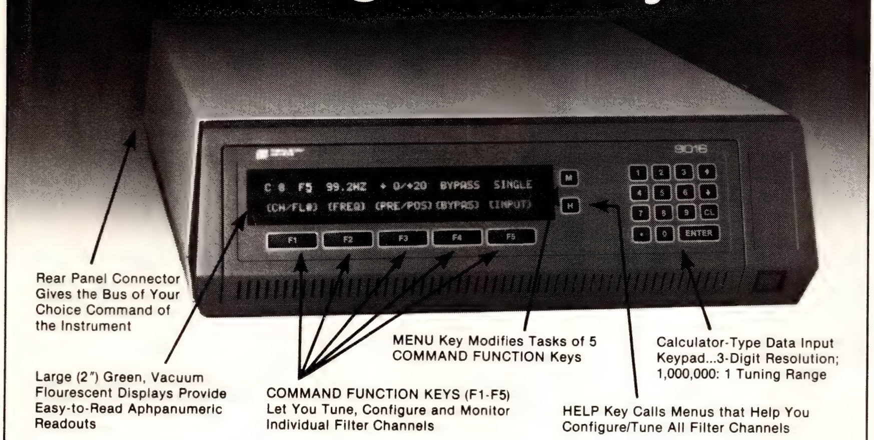
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ers both fun and obligatory. "They teach people analog fundamentals in universities, but in the end, industry is going to have to spend years training these people. There really is no substitute for sitting at a lab bench with a lot of expensive equipment around and having someone hold your hand." He gets several job offers a year, but finds few interesting. "I don't want just a job. I want fun. There's a difference."

Circuits, skiing, and tennis

Despite his passion for circuit design, it remains only part of his life's focus. "I'm not a workaholic, but I don't see a [boundary line] between circuit design and skiing, tennis, or travel. They all seem to fit together nicely. Some people think about skiing while they're at work; I think about circuit design while I'm skiing."

Indeed, he's taken the same immersion approach to learn other activities that he took to learn circuit design. When he wanted to learn to ski, he started with a lesson, but then drifted away from the rest of the class, spending the rest of the week skiing—and falling—down the slopes until he had begun to master the techniques. After completing a course on cooking, he tackled coq au vin at home, making it five nights in a row until it met his approval. When one restaurant's hollandaise sauce struck him as especially well made, he convinced the chef to let him into the kitchen and teach him her techniques.

Out of all the activities he engages in, writing about his designs is the least satisfying. Descriptive articles about circuit design can never recapture the thrill of the design process, he says. "On paper, it's just never good enough. I can never match the level of emotion I feel for a circuit when I see it on paper."

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1987 Editorial Calendar and Planning Guide

EDN

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Mar. 4	Feb. 12	Computer Graphics; Communications ICs; Test & Measurement	Closing: Feb. 26 Mailing: Mar. 16
Mar. 18	Feb. 26	CAE; ASICs; Electro '87; Show & Product Preview	
Mar. 31	Mar. 10	Electro '87 Show Issue; Design & Development Tools; ICs & Semiconductors	
Apr. 15	Mar. 26	Microprocessor Technology; Software Development; Digital ICs	Closing: Apr. 2 Mailing: Apr. 23
Apr. 30	Apr. 9	Communications Special Issue; ASICs; Test & Measurement	
May 14	Apr. 23	Analog Technology Special Issue; ICs; Test & Measurement	Closing: Apr. 30 Mailing: May 21
May 28	May 7	Computer Peripherals; Software; Power Sources/Devices	
June 11	May 21	Math ICs; CAE; Computers	Closing: May 28 Mailing: June 18
June 25	June 4	ASIC (Semicustom ICs) Directory; Analog ICs; Surface-Mount Technology	
July 9	June 18	Product Showcase-Volume 1; ICs & Semiconductors; Software	Closing: June 25 Mailing: July 16
July 23	July 2	Product Showcase-Volume II; Computers & Peripherals; Test & Measurement Instruments	
Aug. 6	July 16	Computer Boards; Digital Signal Processing; Test & Measurement; Top Ten Reader Vote Contest	Closing: July 23 Mailing: Aug. 13
Aug. 20	July 30	Military Electronics Special Issue; Fiberoptics; Software	
Sept. 3	Aug. 13	Analog ICs; CAE; ASICs	Closing: Aug. 20 Mailing: Sept. 10
Sept. 17	Aug. 27	Memory Technology; Communications Technology; Software	
Oct. 1	Sept. 10	Surface-Mount Technology; Computers & Peripherals; Industrial Product Showcase	Closing: Sept. 17 Mailing: Oct. 6
Oct. 15	Sept. 24	Test & Measurement Special Issue; Analog ICs; ASICs	
Oct. 29	Oct. 8	Computers & Peripherals; ICs & Semiconductors; Wescon '87 Product Preview	Closing: Oct. 15 Mailing: Nov. 5
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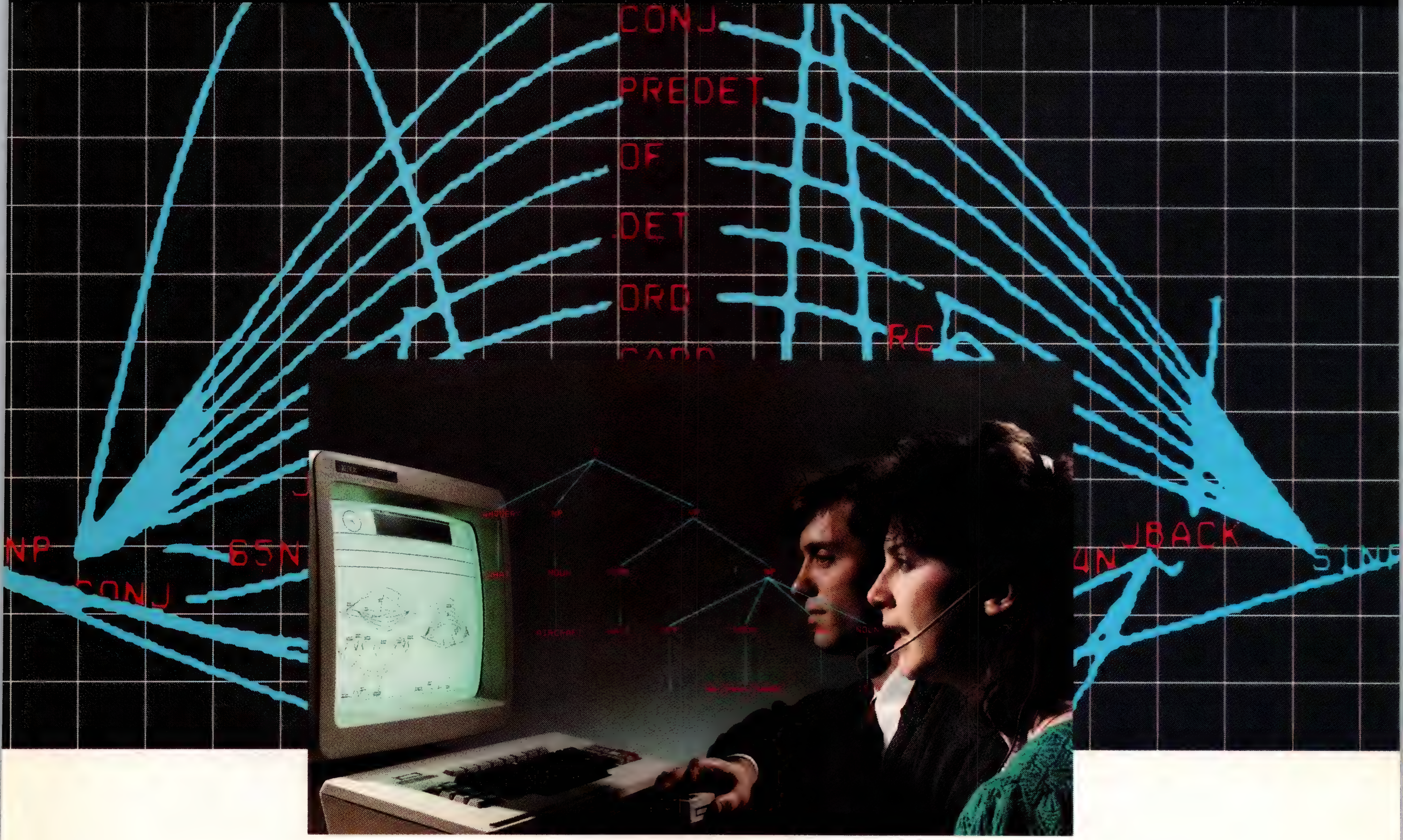

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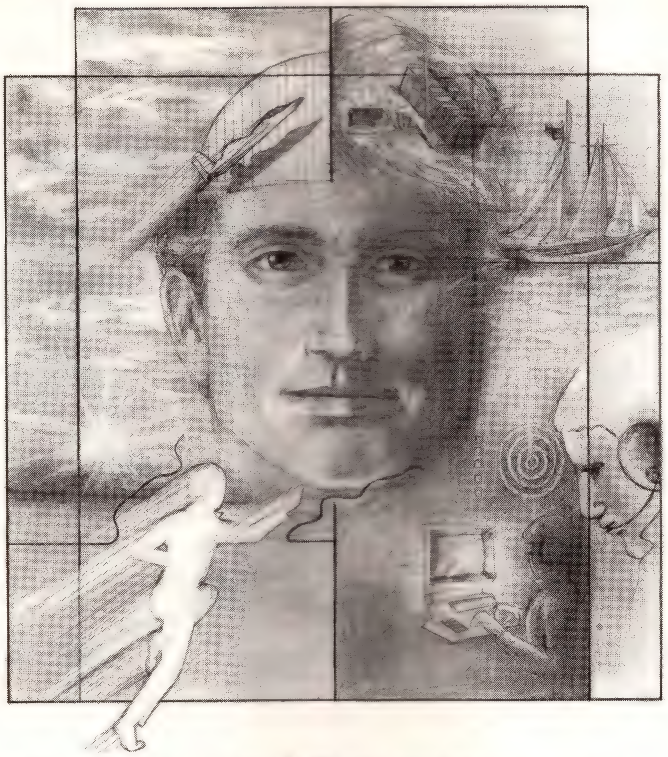

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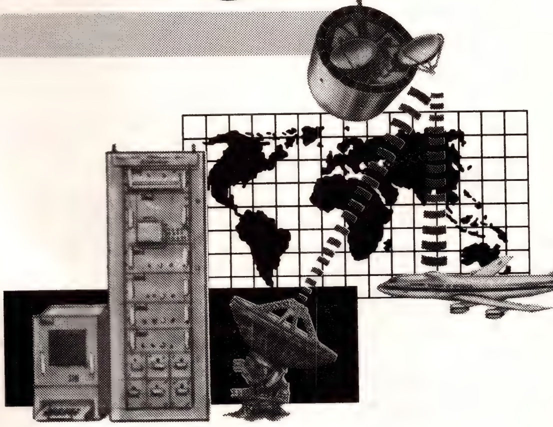

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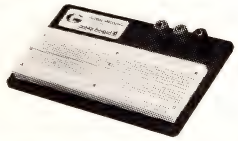

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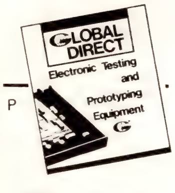

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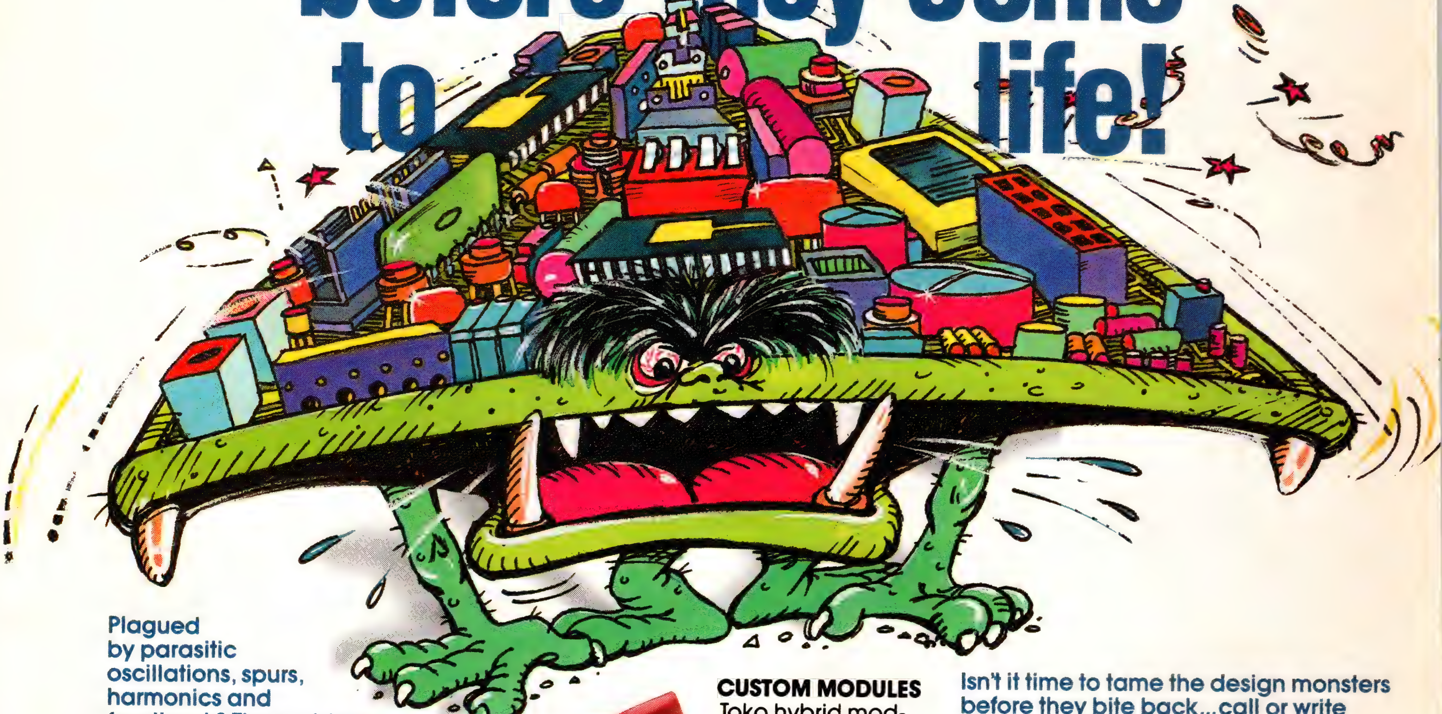

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LOOKING AHEAD

EDITED BY GEORGE STUBBS

US SEMICONDUCTOR MARKET FORECASTS

ORGANIZATION	1986 FORECASTS*	1987 FORECASTS**
SIA	25%	22%
DATAQUEST	10%	12%
ICE	6%	4%
IN-STAT	−2.5%	5%

*RELEASED OCTOBER, 1985
**RELEASED OCTOBER/NOVEMBER, 1986

(SOURCE: ICE CORP)

Analysts' 1987 forecasts vary for US semiconductor sales

Semiconductor-industry analysts have issued the latest round of forecasts for the 1987 US semiconductor market, and once again the predictions vary widely, although not quite as widely as the 1986 forecasts. Once again, the Semiconductor Industry Association is most optimistic about the market, predicting 22% growth. The least optimistic projection is Integrated Circuit Engineering Corp's (Scottsdale, AZ) at 4%.

In making its prediction, ICE has assumed a 3% growth rate in the US production of electronic systems and a "relatively unexciting" overall US economic picture—no recession, no boom, and an approximate 2% GNP growth. Moreover, ICE does not believe that system manufacturers will be inclined to build or rebuild significant levels of semiconductor inventories in 1987.

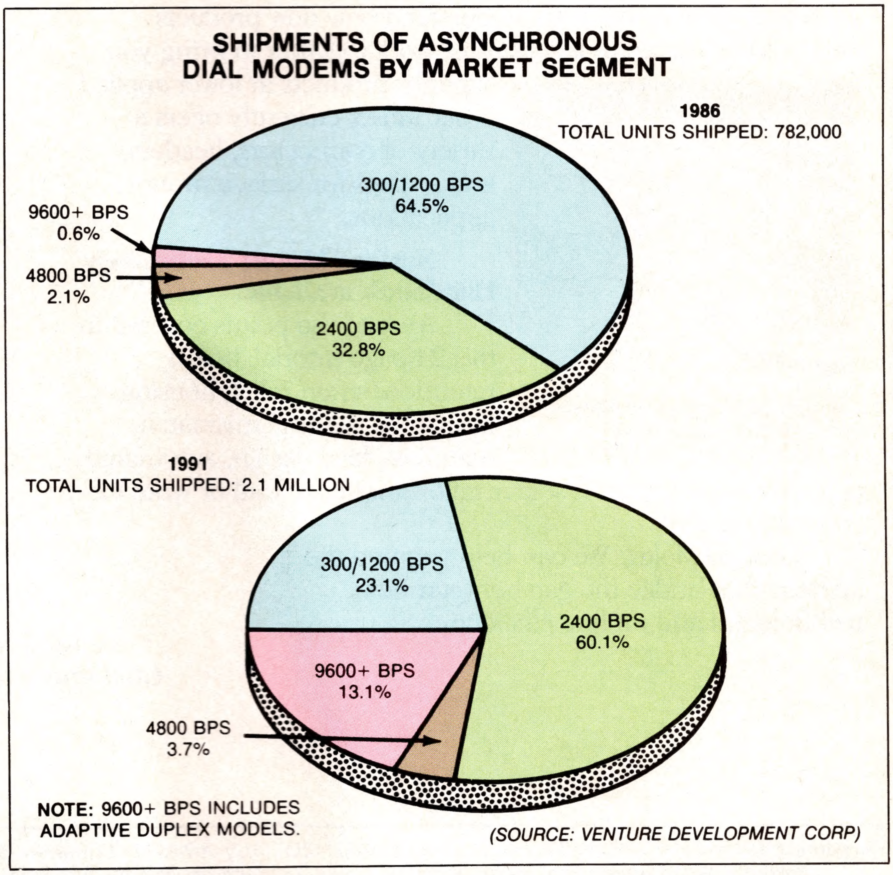
Async dial modems stay on top in units shipped to 1991

Although the modem market continues to change as users demonstrate their preferences for higher speeds and more advanced features, basic asynchronous dial modems will continue to account for the majority of new modems shipped through 1991. So says the market-research company Venture Development Corp (Natick, MA), which also reports that higher-speed models will gain in popularity and that the market share of more sophisticated modems will also be expanding.

Approximately 60% of all modems shipped, from now into the next decade, will be async dial modems. PC-to-PC applications for file transfer and graphics will help maintain the high popularity of these modems. Because the async units are relatively inexpensive, however, the sales value they represent will be roughly 15 to 20% of the total modem sales value. The average annual growth rate of the market for async dial modems through 1991 will be 21.9%.

VDC expects that, within this market segment, 2400-bps modems will become the most popular in terms of units shipped, even as technological advances make 4800- and 9600-bps full-duplex units increasingly attractive. The average annual growth rates for these last two types of modem will still be spectacular at 36.5% and 80%, respectively.

Shipments of synchronous dial modems, which typically operate in half-duplex mode, will grow by approximately 11% annually through 1991, says VDC. As the cost of private lines increases, the market for leased-line modems will grow by almost 24% annually, and high-speed models—14.4k bps and above—will experience exceptional growth.



(SOURCE: VENTURE DEVELOPMENT CORP)

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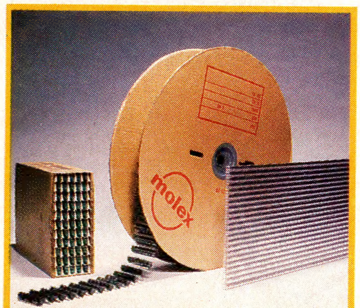

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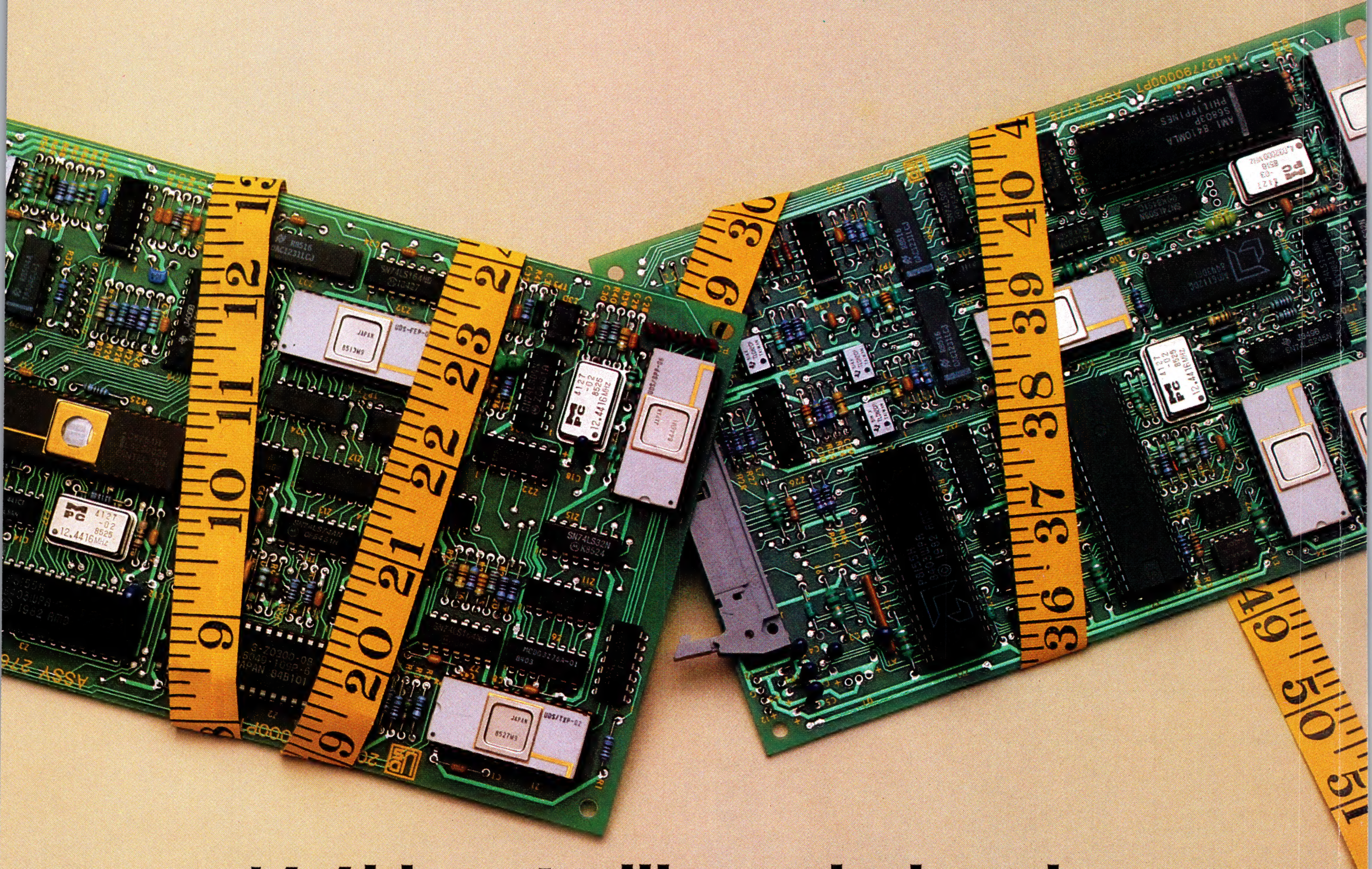

14.4kbps trellis coded and 9.6kbps modems on 40 square inches

LSI technology and UDS engineering expertise have combined to deliver two major improvements in modem design. Two of the most complex modems in the UDS product line — the fast-polling 9600FP and the Trellis Coded 14.4 — have now been reduced to 40 square inches of board space for each complete modem. To accommodate varying OEM configurations, a wide variety of form-factor layouts and option packages is available.

9600FP
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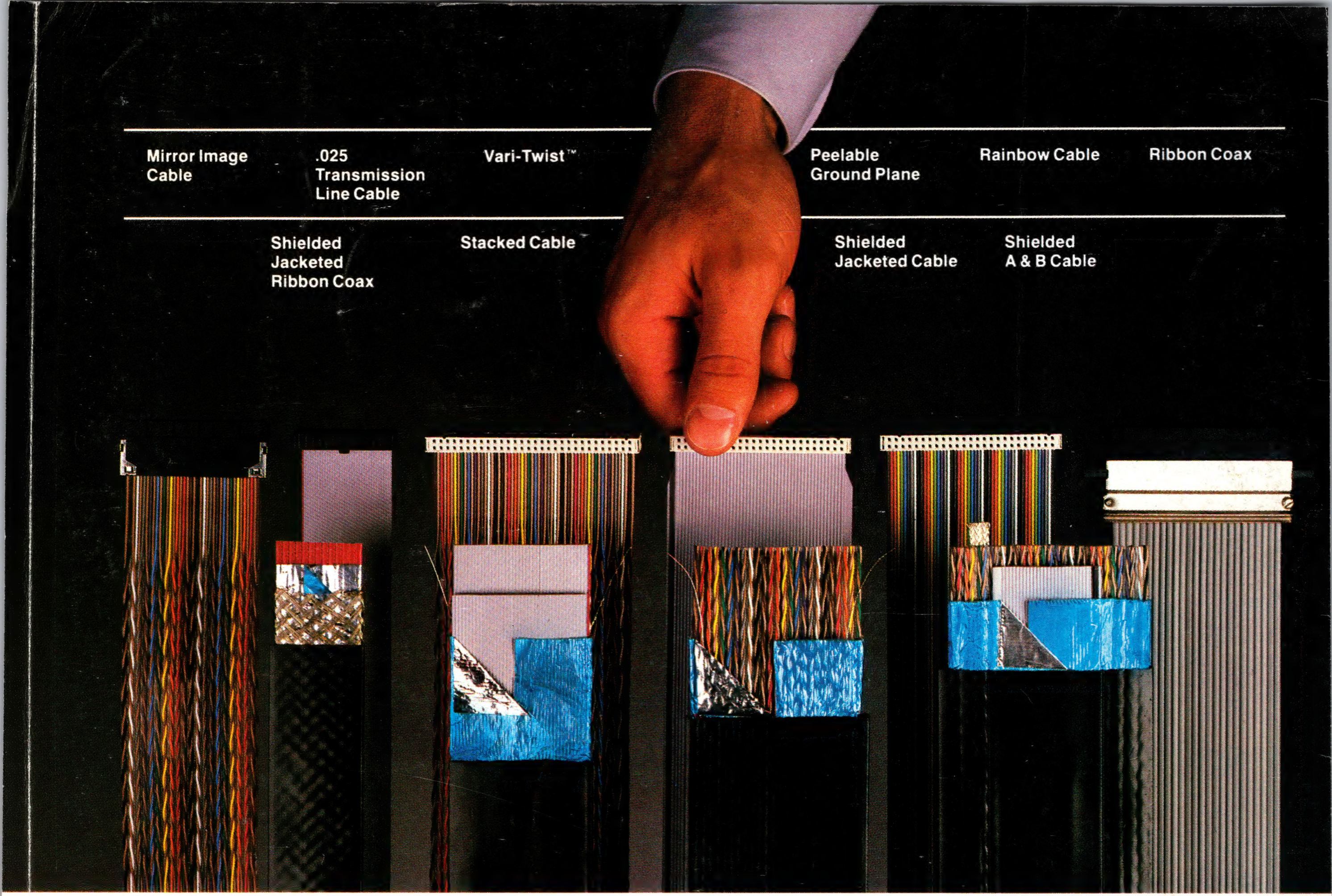

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